# *Charge Nonconservative Ac Modeling of Fgmosfet*

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***Abstract***

This paper studies the Floating- Gate MOSFET (FGMOSFET) for its importance in biomedical engineering and many modern low-power applications. A practical model for FGMOSFET is highly needed to be used in circuits simulators. In this work, a spice model for FGMOSFET is introduced and can be inserted in any circuit simulator such as Spector and various SPICE programs (i.e. HSPICE, WinSPICE, etc.). Firstly, the parasitic capacitances needed for FGMOSFET is revised for 0.13um CMOS technology. Secondly, a model for both mutual and output transconductance is represented. The model is based on n-channel FGMOSFET and valid from linear to saturation regions. The model considers velocity saturation as short channel effect and bulk charge due to drain-to-source voltage as second order effect. The results were verified by the spice simulation BSIM3v3 model in Cadence. The model is not a charge conservative.

**Keywords**— FGMOSFET Model; CAD tools; Devices Modeling; Nano Electronics; Spice Circuit Simulation**.**

## I. INTRODUCTION

COMPUTER AIDED DESIGN (CAD) TOOLS IS CONSIDERED THE BASIC REFERENCE TO CIRCUIT SIMULATION NOWADAYS. IT HELPS RESEARCHERS AND INDUSTRY PEOPLE TO FIGURE OUT THE CHARACTERISTIC FOR THEIR DEVICES IN AN ACCURATE WAY.

FLOATING-GATE MOS DEVICES HAVE BEEN BELIEVED AS ONE OF THE DOMINANT STRUCTURES TO EXTEND THE SCALING LIMIT DUE TO THE INCREASING OF THRESHOLD VOLTAGE CONTROL. THE FGMOS DEVICES ATTRACT THE RESEARCHERS WORKING ON ANALOG DESIGN DUE TO ITS ELECTRICAL CHARACTERISTICS FOR DATA COMPUTATION AND LOW POWER DISSIPATION. MOREOVER, THE FGMOS DEVICES ARE GOOD DEVICES FOR CONTROLLING THRESHOLD VOLTAGE AND ENHANCING THE CHARGING AND DISCHARGING TIME THROUGH THE COUPLING CAPACITANCE VALUE CONTROL. THE FGMOS DEVICES FOLLOW THE SAME CMOS TECHNOLOGY AND DOES NOT NEED A SPECIFIC FABRICATION PROCESS [1].

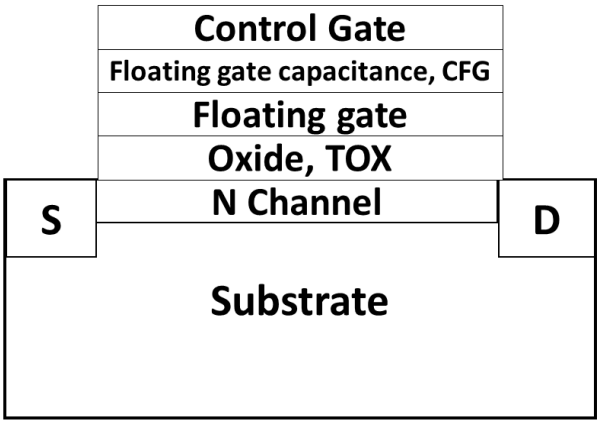


**Fig. 1 Structure of FGMOSFET device.**

Shows the structure of FGMOSFET device where $T_{OX}$ is the thickness of oxide between floating gate and channel and $C_{FG}$ is the capacitance between the control gate and floating gate.

Floating Gate MOSFET (FGMOSFET) is found in many circuits like Flash and EEPROM Memories, low-power circuits [2], many biomedical Sensors like DeFET [3] and photonics circuits [4].

This paper represents a practical model for FGMOSFET to be used in future for circuit and device simulation. The parasitic capacitances are revised [5]. Then a mathematical model for mutual and output transconductance is introduced. Finally, a comparison between the proposed model and BSIM3v3 model [6] in Cadence is discussed. The simulation method [7] is the same as used in [5]. The proposed model is not a charge conservative, unlike BSIM3v3, but is more flexible to use as it doesn't depend on parameter extraction as in the other.

## II. PARASITIC CAPACITANCES

From [5], the parasitic capacitances, $C_{fs}$ and $C_{fd}$, in linear and saturation regions where found to be in the form:

**(1)**

$$C_{fd} = \frac{X_v\left(\frac{k}{E_c}\right)\left(E_c L V_c\left[V_{fd}^{\,2} - 2\alpha_c V_{fd}\left[2\emptyset_p + V_{FB} + \Delta V_{th}\right] - \alpha_c \frac{2}{6}\frac{\gamma}{\sqrt{2\emptyset_p}} V_{DS}^{\,2}\right] - 2X_v V_{fd}\right) - V_{fd} Z}{X_v^{\,2}}$$

**(2)**

Where $C_{fs}$ and $C_{fd}$ are the parasitic capacitances between floating gate and Source and Drain, respectively.

The parameters in the two equations are as following:

1) *K, called the conductivity of FGMOSFET*

$$k = (WC_{ox}/\alpha_c)$$

**(3)**

Where W is the transistor width, $C_{ox}$ is the oxide capacitance between the floating gate and channel and $\alpha_c$ is the capacitance coupling coefficient between the floating gate, and control gate.

2) *$E_c$ the critical electric field.*

3) *L is the transistor length.*

4) *$V_{FB}$ is the flat band voltage due to nonideality of the MOS capacitor.*

5) $\Delta V_{th}$ term represents the Drain Induced Barrier Lowering (DIBL) effect from BSIM4 [8].

6) Other terms represents the voltage of the structure as discussed in [5].

The parasitic capacitance can be used to derive the DC model of FGMOSFET as in [5] and the AC model as discussed in next section.

## III. TRANSCONDUCTANCE MODEL

The main elements which are needed in AC modeling of a transistor are the parasitic capacitances and transconductances. The mutual conductance $g_m$ and output (drain) conductance $g_d$ can be easily derived by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} |V_{DS}$$

**(4)**

$$g_d = \frac{\partial I_D}{\partial V_{DS}} |V_{GS}$$

**(5)**

Where $I_D$ is the drain current derived in [5] and $V_{GS}$ and $V_{DS}$ are control gate and Drain to Source voltages, respectively.

The results of this partial differentiation are:

$$g_m = \frac{\frac{W \mu_{ns} C_{ox}}{L} V_{DS}}{V_c}$$

**(6)**

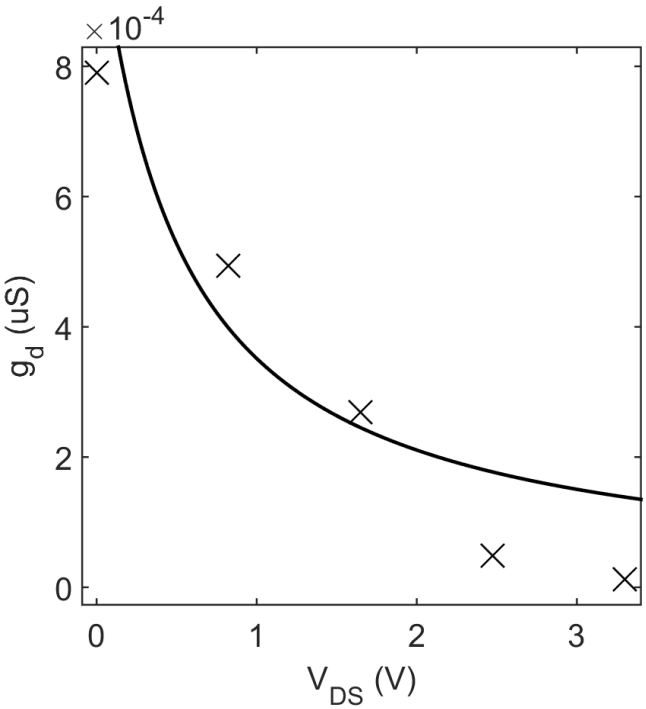


Fig. 2 DC analysis for output transconductance of FGMOSFET in siemens vs. drain to source voltage, solid line is the model and symbol is the BSIM3v3 model in simulator. The control gate voltage equals **2.5V.**

**(7)**

$$g_d = \frac{\frac{W \mu_{ns} C_{ox}}{\alpha_c L}\left[-\alpha_c V_{GS} + X_c V_{DS} + \alpha_c (V_{TO} + V_{FB}) + \frac{X_c}{2 E_c L} V_{DS}^2\right]}{V_c^2}$$

Where $\mu_{ns}$, $V_c$, $V_{TO}$ are the effective surface mobility of electrons [9], the effect of the velocity saturation [5] and threshold voltage at zero drain bias [10]

The term $X_C$ is expressed as:

$$X_c = \alpha_c \frac{\Delta V_{th}}{V_{DS}} + 1 - 2\alpha_d \quad \textbf{(8)}$$

Where $\alpha_d$ is the capacitance coupling coefficient between the floating gate and drain. $\frac{\Delta V_{th}}{V_{DS}}$ represent a constant term for DIBL effect depends on channel length, doping of substrate,

oxide thickness and electric permittivity of oxide and silicon.

As shown in the transconductance equations, they need the values of the parasitic capacitances derived in [5].

## IV. Results Verification

Fig. 2 represents the comparison between the proposed model and the BSIM3v3 simulation in DC simulation in Cadence for output conductance.

The parasitic capacitance values in [5] were used to draw the model of the transconductances. Then simulation for FGMOSFET in Cadence were done. Finally, both model and simulation were put in one figure for comparison

There is a difference between the proposed model and BSIM3v3 and this is because the proposed model is a charge nonconservative

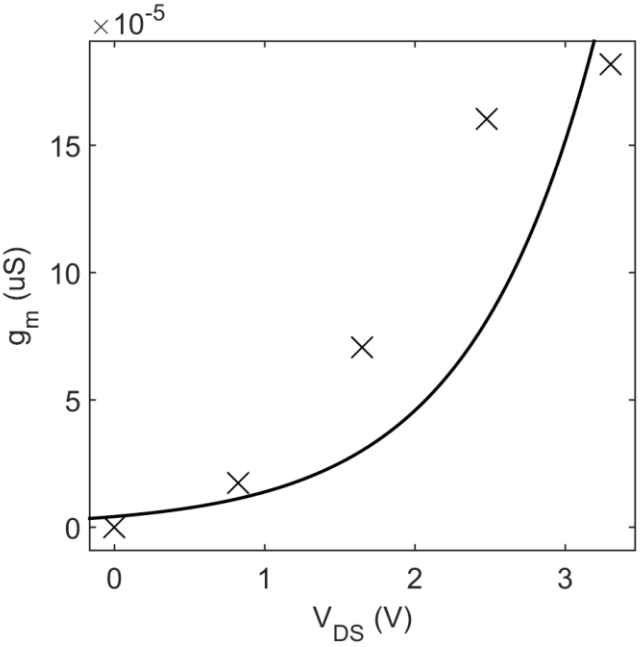


Fig. 3 DC analysis for mutual transconductance of FGMOSFET in siemens vs. drain to source voltage, solid line is the model and symbol is the BSIM3v3 model in simulator. The control gate voltage equals 2.5V.

model while BSIM3v3 is not. The percentage of error in best cases is 5%.

Fig. 3 shows the comparison between the proposed model and the BSIM3v3 simulation in DC simulation in Cadence for mutual conductance.

All parameters used are stated in Table. 1.

TABLE I. PARAMETERS USED

| **Parameter** | **Symbol** | **Value** |
|---|---|---|
| Oxide thicknes | $T_{OX}$ | 3 nm |
| Relative permittivity of silicon oxide | $\epsilon_{r,ox}$ | 3.9 |
| Transistor width | W | 1 um |
| Transistor length | L | 340 nm |
| Floating gate capacitance | $C_{FG}$ | 2.4 fF |

The same simulation method [7] for FGMOSFET that used in [5] is used here, see Fig. 4.

**CONCLUSION**

In this work, mathematical modeling of transconductances of FGMOSFET is stated. The model is practical and can be used in many circuit simulators. The main disadvantage of the proposed model is that it is charge independent model. So, the model is not very accurate with error percentage of 5% in

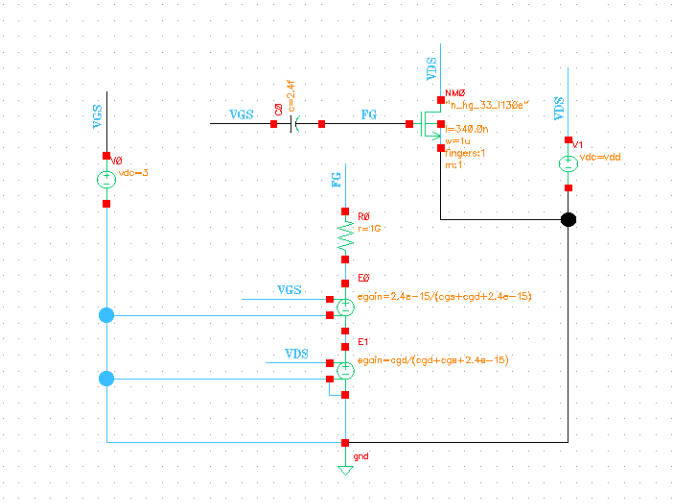


**Fig. 4 Cadence schematic diagram for simulating FGMOSFET with BSIM3v3 model.**

most values along the sweep with voltage. The error percentage is also bad for using less efficient mobility model.

Future intention is to adapt this model for short-channel devices at sub 100nm and make a charge conservative model for the parasitic capacitances of FGMOSFET and correspondingly for the transconductances. The enhanced models in future will be added to any circuit simulator that support Verilog-A or Spice syntax.

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