ISSN 2347-3487

Influence of annealing temperature on the electrical, structural and surface morphology properties of Au/Cr Schottky contacts on n-type InP

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ABSTRACT

The influence of rapid thermal annealing on the electrical and structural properties of Au/Cr/n-InP Schottky diode have been investigated by the current-voltage (I-V), capacitance-voltage (C-V), auger electron spectroscopy (AES) and X-ray diffraction (XRD) measurements. The Schottky barrier height (SBH) and ideality factor (n) of the as-deposited Au/Cr/n-InP Schottky diode are 0.51 eV (I-V)/0.64 eV (C-V) and 1.81, respectively. When the contact is annealed at 200 ^{o}C in N_2 atmosphere for 1min, a maximum SBH (0.71 eV (I-V)/0.81 eV (C-V)) and low ideality factor (1.15) are achieved for the Au/Cr/n-InP Schottky diode. However, after annealing at 300 ^{o}C, the SBH slightly decreases to 0.58 eV (I-V)/0.69 eV (C-V), and ideality factor increases to 1.45, respectively. The SBHs obtained from the Norde and Cheung's methods are closely matched with those obtained from the I-V method. Results show that the optimum annealing temperature for the Au/Cr/n-InP Schottky diode is 200 °C. Further, the discrepancy between SBHs calculated from I-V and C-V methods is also discussed. Moreover, the energy distribution of interface state density is estimated from forward bias I-V characteristics at different annealing temperatures. AES and XRD studies reveal that the formation of indium (In) phases at Au/Cr and InP interface may be the cause for the increase in SBH after annealing at 200 ^{o}C. The AFM results show that the overall surface morphology of Au/Cr Schottky contacts is considerably smooth at elevated temperatures.

Indexing terms/Keywords

n-type InP, Au/Cr Schottky contacts, Barrier heights, Auger electron spectroscopy, X-ray diffraction studies .

Academic Discipline And Sub-Disciplines

Microelectronics, Metal-semiconductor (MS) contacts

SUBJECT CLASSIFICATION

Semicondutor Physics, Electrical properties

TYPE (METHOD/APPROACH)

Rapid thermal annealing, current-voltage (I-V) and capacitance-voltage (C-V) measurements, Auger electron spectroscopy depth profile, X-ray diffraction measurements, atomic force microscopy.

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Council for Innovative Research
Peer Review Research Publishing System
Journal: JOURNAL OF ADVANCES IN PHYSICS
Vol 5, No.3
japeditor@gmail.com
www.cirjap.com

ISSN 2347-3487

1.INTRODUCTION

III-V compound semiconductor, especially indium phospide (InP) has received much attention for the fabrication of optoelectronics, microwave devices, integrated circuits used in modern high-speed optical communications and Schottky junctions etc. [1-5]. This is due to direct energy band gap, high electron mobility, radiation hardness and high saturation drift velocity. The Schottky diode is a fundamental component in solid state electronics and has received extensive attention over the few decades. The performance and reliability of Schottky barrier diodes (SBD) strongly depend on the MS interface. Hence it is important to have a full understanding of the reactions of metal contacts with InP. Therefore, the fabrication of high-quality, more reliable Schottky contacts to InP with high barrier height, low-leakage current and good thermal stability is still a challenge. Generally InP Schottky diodes show low barrier height (BH) than desirable due to many reasons. One of them may be the out diffusion of InP atoms into the deposited metal films leaving vacancies or defects within the band gap pinning the Fermi level [6].

Various metal schemes have been used for the formation of Schottky rectifiers on n-InP by many research groups. For example, Cetin et al. [7] prepared Au and Cr/n-InP Schottky barrier diodes and reported that the effective barrier height of the Au and Cr contacts were 0.480 eV, 0.404 eV and 0.524 eV, 0.453 eV from current-voltage (I-V) and capacitance–voltage (C-V) measurements, respectively. Huang et al.[8] studied a high performance of bilayer Pt/Al contacts on n-InP and found to be the effective barrier height of 0.74 eV and ideality factor of 1.11. Reddy et al. [9] investigated the electrical, structural and morphological characterstics of rapidly annealed Pt/Ti double metal structure on n-InP and reported that increase or decrease in Schottky barrier height upon annealing at elevated temperatures could be attributed to the formation of interfacial phases at Pt/Ti interface according to AES and XRD results. Devi et al. [10] investigated the electrical and structural properties of Au/Cu Schottky contacts on n-InP as a function of annealing temperature. They reported that the barrier height increased (0.82 eV (I-V) and 1.04 eV (C-V)) after annealing at 400 ^{o}C and decreased (0.75 eV (I-V), 0.88 eV (C-V) upon annealing at 600 ^{o}C. Huang and Horng [11] studied the electrical and structural properties of Pt/Al/n-InP Schottky diodes and reported that the double metal contact structure provides better rectification characteristics than single metal/n-InP Schottky diodes. Reddy et al. [12] investigated the annealing effect on electrical properties and interfacial reactions of Ni/Cu Schottky rectifiers on n-InP. They found that the barrier height decreased with annealing temperature compared to the as-deposited one. Bhaskar Reddy et al. [13] prepared the Au/Ni/n-InP Schottky barrier diode and reported that the barrier heights were effectively influenced by rapid thermal annealing. Naik et al. [14] investgated the electrical and structural properties of Pd/V/n-InP Schottky structure as a function of annealing temperature. They reported that the increase in barrier height after annealing at 200 ^{o}C might be due to the formation of indium (In) phases at interface vicinity. Recently, Yatskiv et al. [15] prepared Pt/InP Schottky contact by electrophoretic deposition of Pt nano particles and studied its electrical properties at different temperatures.

Our main objective of this work is to fabricate and characterize the Au/Cr Schottky contacts on n-InP as a function of annealing temperature. As far as we know, no one has investigated the electrical, structural and surface morphological properties of Au/Cr/n-InP Schottky contact at different annealing temperatures. In the present work chromium (Cr) is selected as the first layer since it has low work function as well as to provide the low forward voltage drop. Gold (Au) is used as the second layer in order to prevent oxidation as well as to promote current spreading in the contact and good smoothness to the contact. In this work, we investigate the electrical, structural and morphological properties of Au/Cr Schottky contact on n-type InP at different annealing temperatures. Using various analysis techniques (Forward I-V, C-V, Cheung and Norde methods), the diode parameters such as barrier height (Φ_b), ideality factor (n), series resistance (R_s), and interface state density (N_{ss}) are calculated and discussed. Also, the interface analysis of Au/Cr/n-InP Schottky diode is investigated by auger electron spectroscopy (AES) depth profile and X-ray diffraction (XRD) measurements at different annealing temperatures.

2.EXPERIMENTAL DETAILS

Liquid Encapsulated Czochralski (LEC) grown undoped n-InP (100) samples with carrier concentration of $5\times10^{15}cm^{-3}$ were used in the present work. The wafers were initially degreased with organic solutions like trichloroethylene, acetone and methanol by means of ultrasonic agitation for 5 min in each stage to remove the contaminants followed by rinsing in deionised water and then dried in N_2 flow. Further, the samples were etched with HF (49%) and H_2O (1:10) to remove the native oxides from the wafer surface. Finally, the wafers were rinsed in deionised water. Ohmic contact on back side of the InP wafer was formed by deposition indium (In) metal (500Å) followed by rapid thermal annealing at 350 ^{o}C in N_2 atmosphere for 1min. The metals Au/Cr (300/200 Å) layers were deposited on the polished side of the InP wafer with a diameter 0.7mm through a stainless- steel mask using a e-beam evaporation system. All evaporations process were carried out under a vacuum pressure of 5×10^{-6}mbar. Sequentially, Schottky contacts were annealed at 100 ^{o}C, 200 ^{o}C and 300 ^{o}C under nitrogen ambient using a rapid thermal annealing (RTA) system. The current–voltage (I-V) and capacitance-voltage (C-V) characteristics of the Au/Cr Schottky contacts to n-InP were measured using a Keithley-source measuring unit (Model No 2400) and automated deep level spectrometer (SIMILAB DLS-83). To examine the intermixture of the Au/Cr metals with InP before and after annealing, auger electron spectroscopy (AES: UG: micro lab 350) depth profile was used. X-ray diffraction studies (Siefert XRD PW 3710) using Cu Kα radiation) were made to characterize the interfacial reaction between the InP and Au/Cr metal layers. Finally, atomic force microscopy (AFM) (Model No: a MOD-1M plus, Make: Nano focus; Operating mode: Non-contact, tip size <10 nm) was also employed to characterize the surface morphology of the Au/Cr Schottky contacts before and after annealing temperature.

3.RESULTS AND DISCUSSION

3.1 The Current-Voltage (I-V) Characteristics

The forward and reverse bias I-V characteristics of Au/Cr/n-InP Schottky diodes are shown in Figure 1 as a function of annealing temperature. The leakage current of the as-deposited and annealed Au/Cr/n-InP Schottky diode at 100 ^{o}C are measured to be 9.961×10^{-6} A and 8.001×10^{-8} A at -1V. However, for the contact annealed at 200 ^{o}C, the leakage current slightly decreases to 5.373×10^{-9} A at -1V. Further, with the increase in annealing temperature up to 300 ^{o}C, the leakage current increases to 8.079×10^{-7} A at -1V compared to the annealed at 100 ^{o}C and 200 ^{o}C contacts. Experimental results indicate that the electrical properties of Au/Cr/n-InP Schottky diodes are improved after annealing at 200 ^{o}C. According to the thermionic emission (TE) theory, the current through a Schottky barrier diode (SBD) with the series resistance (R_S) at a forward bias *(V≥3kT/q)* and is given by [1]

$$I = I_0 \exp\left(\frac{q(V - IR_S)}{nk_BT}\right)\left[1 - \exp\left(\frac{-q(V - IR_S)}{k_BT}\right)\right] \quad (1)$$

where I is measured current, V is applied voltage, the term IR_s is the voltage drop across the R_s of the diode, k_B is the Boltzmann's constant, n is ideality factor, I_o is reverse saturation current derived from the straight line of intercept of ln(I) at zero bias and it is given by

$$I_o = AA^*T^2 \exp\left(\frac{-q\Phi_b}{k_BT}\right) \quad (2)$$

where A is the effective area of Schottky contact, A* is the effective Richardson constant (the theoretical value of A^* was 9.4 $Acm^{-2}K^{-2}$ for n-InP [16]), q is the charge of electron, T is the absolute temperature and Φ_b is the barrier height and is determined from the extrapolated I_o and is given by

$$\Phi_b = \frac{k_BT}{q}\ln\left(\frac{AA^*T^2}{I_O}\right). \quad (3)$$

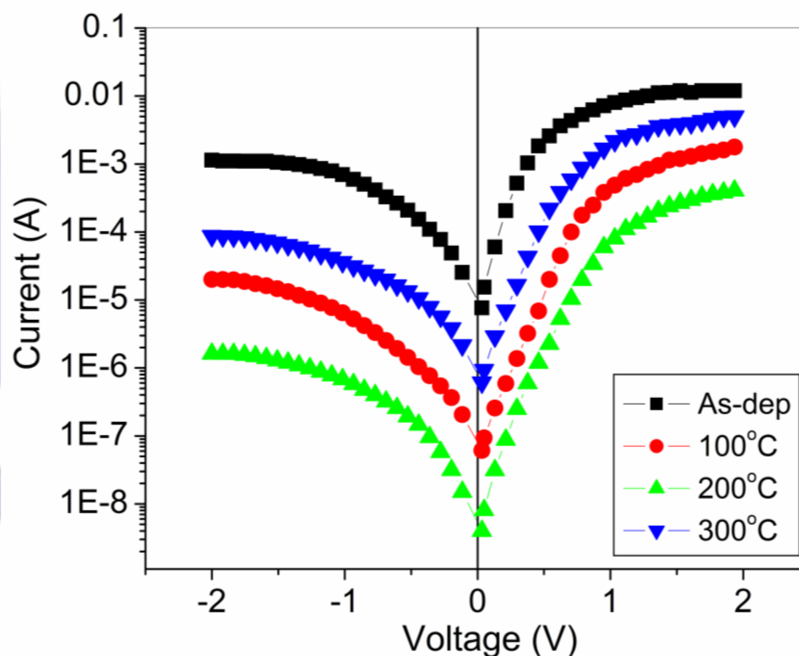


Figure 1.The reverse and forward (I-V) characteristics of the Cr/Au/n-InP Schottky diodes at different temperatures.

The experimental values of Schottky barrier height (SBH) of the as-deposited and 100 ^{o}C annealed contacts are found to be 0.51 eV and 0.63 eV respectively. However, the SBH increases to 0.71 eV for the contact annealed at 200 ^{o}C. Further, the SBH slightly decreases to 0.58 eV when the contact is annealed at 300 ^{o}C. These results indicate that the optimum annealing temperature for the Au/Cr/n-InP Schottky diodes is 200 ^{o}C. According to Duboz et al [17], the lower value of the barrier height for the sample annealed at higher temperature can be attributed to reduction in the density of interfacial defects. The modification of the defect density by annealing could change the pinning at the Fermi level resulting change in the barrier heights. The values of ideality factor *n* can be calculated from the slope of the linear region of the forward I-V characteristics for small forward bias currents where the series resistance is negligible. The ideality factor is given by

$$n = \left(\frac{q}{k_B T}\right)\left(\frac{dV}{d(\ln I)}\right) \quad (4)$$

The ideality factor of as-deposited and annealed at 100 °C the Cr/Au/n-InP Schottky diodes are found to be 1.81 and 1.28 respectively. However, the ideality factor is improved to 1.15 for the contact annealed at 200 °C. Further, the ideality factor slightly increases to 1.45 for the contact annealed at 300 °C. It is noted that the ideality factor is greater than unity for all diodes. This non-ideal behavior can be attributed to (i) defect states in the band gap of the semiconductor providing other current transport mechanism such as barrier tunneling or generation, recombination in the space charge region [18], (ii) laterally inhomogeneous contacts [19] and (iii) interface dipoles caused by an interface and also fabrication induced defects at the interface. The deviation from linearity at higher voltage in the semi logarithmic *I–V* characteristics is due to the series resistance, the interface layer and interface states of the structures [20].

As it can be seen from Figure 1, at low forward bias voltages, the forward bias I-V characteristics are linear on a semi-log-artimatic scale but deviate considerably from linearity which may be due to the effect of series resistances (R_s), the interface layer, and the interface states when the applied voltage is significantly large. The series resistance (R_s) is important in the downward curvature of the forward bias I-V characteristics, but the other two Schottky parameters such as barrier height Φ_b and ideality factor *n* are significant in both the linear and non-linear regions of the *I-V* characteristics. As the linear range of the forward *I-V* plots is reduced, the accuracy of the determination of SBH and ideality factor becomes smaller. Therefore Φ_b, n and R_s are also estimated from the downward curvature of the forward I-V plot, using Cheung's method [21]. Cheung's functions can be expressed as

$$\frac{dV}{d(\ln I)} = IR_S + n\left(\frac{k_B T}{q}\right) \quad (5)$$

$$H(I) = V - n\left(\frac{k_B T}{q}\right)\ln\left(\frac{I}{AA^* T^2}\right) \quad (6)$$

and H(I) can also be written as $H(I) = IR_S + n\Phi_b$ (7)

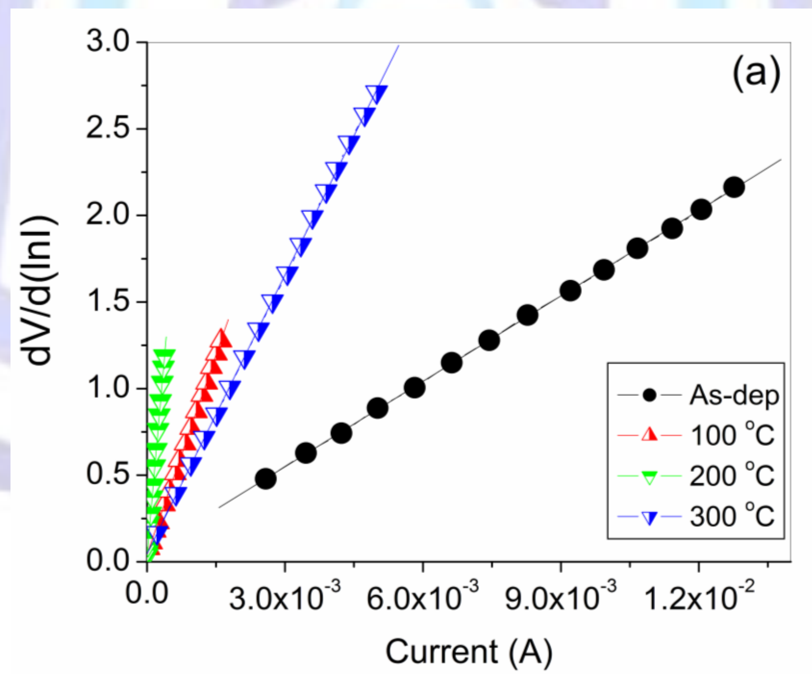


Figure 2. (a) plot of dV/d(lnI) versus I for the Cr/Au/n-InP Schottky diode annealed at different temperatures.

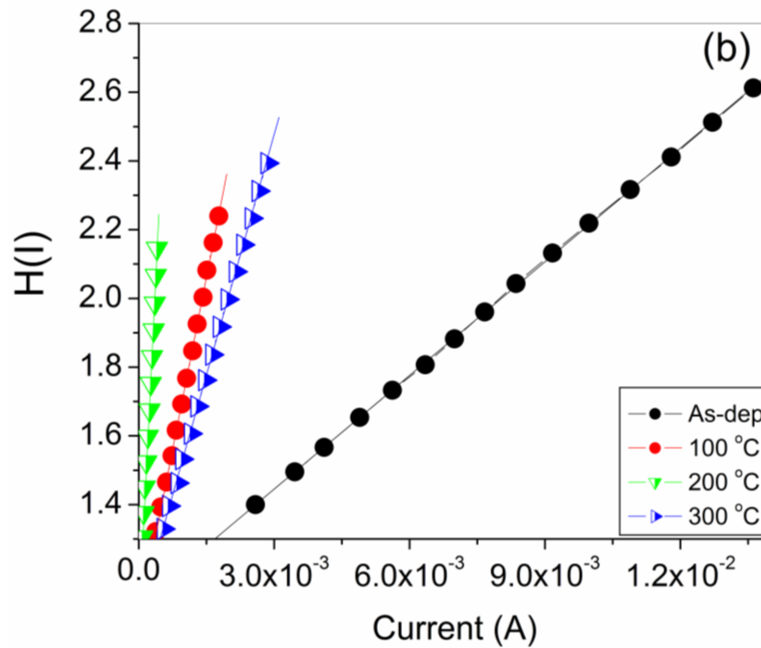


Figure 2. (b) plot of H(I) versus I for the Cr/Au/n-InP Schottky diode annealed at different temperatures.

Figure 2(a) and 2(b) show the experimental dV/d(lnI) versus I and H(I) versus I plots for the as-deposited Au/Cr/n-InP Schottky diode and annealed at 100, 200 and 300 °C respectively. The plot of dV/d(lnI) is linear whose slope gives R_s and the y-axis intercept gives nkT/q from equation (5). The estimated R_s and n values are 164 Ω and 2.14 for as-deposited, 768 Ω and 1.63 for 100 °C, 3022 Ω, 1.47 for 200 °C and 536 Ω, 1.86 for 300 °C. The plot of H(I) versus I must be linear according to equation (7) as shown in Figure 2 (b). The slope of H(I) versus I gives a second method to determine the R_s by using the value of n from equation (6), the Φ_b cab be estimated from the y-intercept of H(I) versus I. The determined values of R_s and Φ_b from H(I) versus I plot are 110 Ω, 667 Ω, 2692 Ω, and 465 Ω, and 0.52 eV, 0.65 eV, 0.71 eV, and 0.58 eV for as-deposited and 100 °C, 200 °C, and 300 °C annealed contacts respectively. These observations revealed that both the R_s obtained from dV/d(lnI) versus I plot and H(I) versus I are in good agreement with each other, implying their consistency and validity.

In order to determine the effective SBH and series resistance (R_s) of Au/Cr/n-InP Schottky diodes, the modified Norde function was also used [22]. In this method a function F(V) is plotted against the V (plot not shown here) and is given by

$$F(V) = \frac{V}{\gamma} - \frac{1}{\beta}\ln\left[\frac{I(V)}{AA^*T^2}\right] \tag{8}$$

where γ is the integer (dimensionless) greater than ideality factor *n* and I(V) is the current obtained from the forward bias I-V curve. The effective SBH (Φ_b) is given by

$$\Phi_b = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q} \tag{9}$$

where $F(V_{min})$ is the minimum point of F(V) and V_{min} is the corresponding voltage. The value of series resistance (R_s) is also determined by the norde function and is given by

$$R_s = \frac{k_B T(\gamma - n)}{qI} \tag{10}$$

The extracted SBH and series resistance (R_s) of the Au/Cr/n-InP Schottky diode are 0.53 eV, 320 Ω for as-deposited, 0.66 eV,199 kΩ for 100 °C, 0.73 eV, 272 kΩ for 200 °C, and 0.60 eV, 15 kΩ for 300 °C respectively. It is observed that there is a good agreement among the values of Φ_b obtained from the forward bias I-V, Cheung's and Norde's methods. Also, series resistance (R_s) estimated by the Norde's method is comparable to that of the Cheung's method.

ISSN 2347-3487

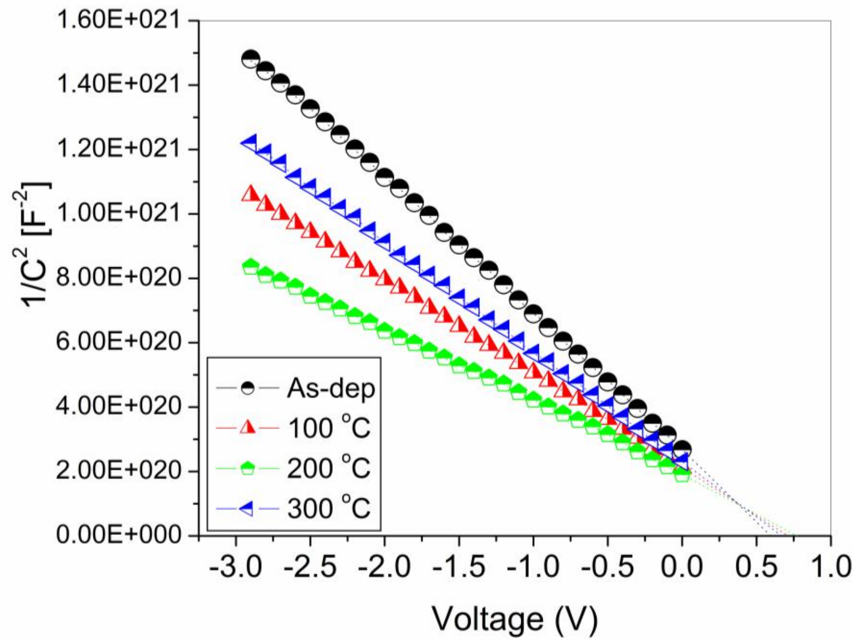


Figure 3. plot of 1/C^2 versus V for the Cr/Au/n-InP Schottky diodes annealed at different temperatures

Capacitance-voltage (C-V) characteristics of the Au/Cr/n-InP Schottky diode are measured at 1MHz in the dark at room temperature. Figure 3 shows a plot of 1/C^2 as a function of bias voltage (V) for the as-deposited and annealed Au/Cr/n-InP Schottky diode. The relationship between the capacitance and the applied voltage in Schottky diodes is given by [1,23]

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_s q N_d A^2}\right)\left(V_{bi} - \frac{kT}{q} - V\right) \tag{11}$$

where ε_s is the permittivity of the semiconductor (ε_s= 9.4 ε_o, where ε_0 is the vacuum permittivity) of n-InP, N_d is the donor concentration, A is the area of the Schottky contact and V_{bi} is the flat band voltage respectively. The x-intercept of (1/C^2) versus V plot yields V_o and V_o is related to the built-in potential V_{bi} by the equation $V_{bi} = V_o + kT/q$, where T is the absolute temperature. The barrier height (Φ_b) is given by $\Phi_b = V_{bi} + V_n$, where $V_n = (kT/q)\ln(N_c/N_d)$.The effective density of states in the conduction band edge is given by $N_c = 2(2\pi m^*kT/h^2)^{3/2}$, where m*= 0.078$m_o$ and its value is 5.7×10^{17} cm^{-3} for InP [24] at room temperature. The SBH of as-deposited Au/Cr/n-InP Schottky diode is found to be 0.64 eV. The estimated SBHs are 0.75 eV for 100 °C, 0.81 eV for 200 °C and 0.69 eV for 300 °C annealed Au/Cr/n-InP Schottky diodes respectively.

Table 1: The electrical parameters of Au/ Cr/n-InP Schottky diode as a function of annealing temperature.

Sample	Schottky barrier height (Φ_b) eV		Ideality factor from I-V	Cheung's functions				Norde		Interface state density
				dV/d(lnI) vs. I		H(I) vs. I				
	I-V	C-V	n	R_s (Ω)	n	R_s (Ω)	(Φ_b) eV	R_s (Ω)	(Φ_b) eV	N_{ss} (eV^{-1}cm^{-2})
As-dep	0.51	0.64	1.81	164	2.14	110	0.52	320	0.53	2.0212x10^{12}
100°C	0.63	0.75	1.28	768	1.63	667	0.65	199 kΩ	0.66	1.0623x10^{12}
200°C	0.71	0.81	1.15	3022	1.47	2692	0.71	272 kΩ	0.73	7.6212x10^{11}
300°C	0.58	0.69	1.45	536	1.86	465	0.58	15 kΩ	0.60	1.4918x10^{12}

A summary of the basic electrical parameters of Au/Cr/n-InP Schottky diodes calculated from *I–V* and *C–V* characteristics at different annealing temperature is given in Table 1. As it can be seen from Table 1 that the barrier heights ($\Phi_{b(I-V)}$) achieved from I-V measurements are significantly lower than those obtained from C-V measurements ($\Phi_{b(C-V)}$). Various authors have reported the reasons for the difference in SBHs obtained from I-V and C-V measurements (in the literature) [25-28]. Based on Hacke et al. [25], the presence of a native oxide layer at the metal-semiconductor interface can cause the discrepancy between the measured $\Phi_{b(I-V)}$ and $\Phi_{b(C-V)}$. According to Song et al. [26] the inhomogeneity in the interface layer composition, non-uniformity of the interfacial layer thickness, and distribution of interface charges can also cause such differences in the SBH estimated from I-V and C-V measurements. Further, the surface damage at the metal-

semiconductor interface affects the I-V measurements because defects may act as recombination centers for trap assisted tunneling currents according to Fontaine et al. [27]. One more possibility is that the product of reactions may not be uniform at the interface at a high annealing temperature. The type and reaction phases may vary from one location to another which cause different SBHs [28].

At high current region, there is always a deviation of the ideality factor which may be due to the presence of a interfacial layer between metal and semiconductor, interface states and series resistance. Thus, for estimating SBH and other characteristic parameters, the interface states play an important role in the semiconductor rectifying contacts. It is well known that for a metal/semiconductor diode having interface states in equilibrium with the semiconductor, the ideality factor *n* becomes greater than unity [29]. The expression of the density of interface states proposed by Card and Rhoderick is given by [29]

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_S}{W_D}\right] \quad (12)$$

where $\varepsilon_i = 3.5\varepsilon_o$ and $\varepsilon_s = 9.4\varepsilon_o$ are the permittivity of the interfacial layer and semiconductor, N_{ss} is the interface state density, δ is the thickness of the interfacial layer and W_D is the width of the space charge region. Further, in n-InP semiconductor the energy of interface states (E_{ss}) with respect to the bottom of the conduction band at the surface of the semiconductor is given by [30,31,32].

$$E_C - E_{SS} = q(\Phi_e - V) \quad (13)$$

where E_{ss} is the energy corresponding to the bottom of the conduction band at the surface of the semiconductor and Φ_e is the effective barrier height, which depends on the applied bias due to an interfacial layer and is given by [33].

$$\Phi_e = \Phi_{bo} + \left(1 - \frac{1}{n}\right)V \quad (14)$$

Thus, Eqs. (12)-(14), along with the I-V characteristics can be used for estimation of interface state density (N_{ss}) as a function of interface state energy (E_{ss}). The N_{ss} versus E_c-E_{ss} plot of the Au/Cr/n-InP Schottky diode is shown in Figure 4.

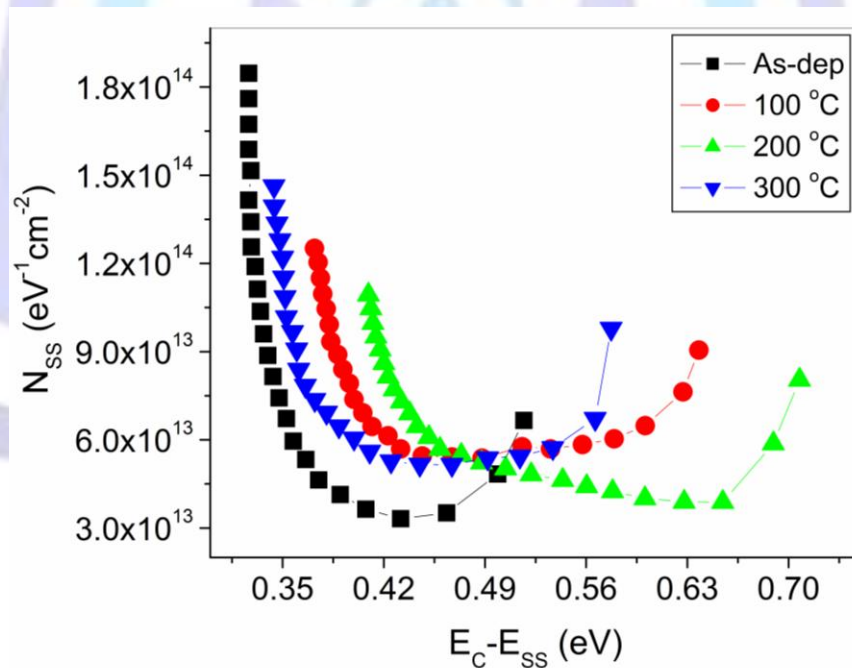


Figure 4. Density of interface states N_{ss} as a function of E_c-E_{ss} for the Cr/Au/n-InP Schottky diodes at various temperatures.

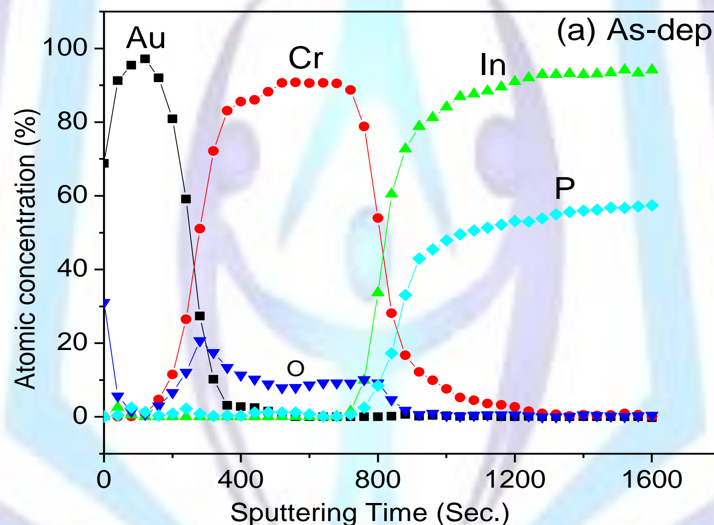
It can be seen from Figure 4, an experimental increase in interface state density exists from mid gap towards the bottom of the conduction band is very apparent, and N_{ss} values obtained decreases with an increase of applied voltages. The value of interface state density is estimated for the as-deposited Au/Cr/n-InP Schottky diode is 2.021×10^{12} $eV^{-1}cm^{-2}$. For the contacts annealed at 100 °C, 200 °C, and 300 °C, the interface state densities are 1.062×10^{12} $eV^{-1}cm^{-2}$, 7.621×10^{11} $eV^{-1}cm^{-2}$, and 1.4918×10^{12} $eV^{-1}cm^{-2}$ respectively. The results of the alone has explained that the increase in annealing temperature up to 200 °C the values of interface state density are decreased and then slightly increased after annealing at 300 °C. The change in the charge of the interface states and thus the interface state energy distribution due to the

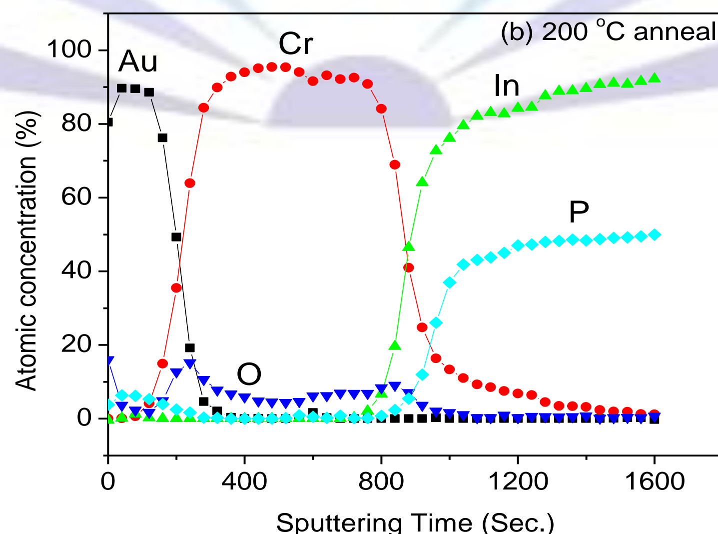
ISSN 2347-3487

potential drop across the interfacial layer varies with the bias. It alters the diffusion potential and therefore the depletion capacitance [1,24,33]. The expermental results show that the interface states density (N_{ss}), and series resistance (R_s) has a significant effect on the electrical characteristics of the Schottky device.

3.2 Structural and Morphological Characteristics

AES depth profile measurement was employed to examine the variation in the BHs of the Au/Cr/n-inP Schottky diode before and after annealing at 300 ^{o}C in N_2 ambient for 1 min. AES depth profiles of the as-deposited and annealed at 200 ^{o}C and 300 ^{o}C are shown in Figure 5. The atomic concentration percentage is recorded as a function of sputtering time to investigate the interfacial reaction between Au/Cr metal layers and InP film. The as-deposited layers Au/Cr, Figure 5(a), exhibit a relative sharp interface indicating that there is no significant inter-diffusion (or) out diffusion between the Au/Cr metal layers and InP layer. When the contact annealed at 200 ^{o}C, Figure 5(b) AES depth profile of the Au/Cr contact shows that indium (In) is out diffused into Au/Cr film this leads to the possibility of a reaction between Au/Cr and In film, resulting in the formation of Cr-In and Au-In interfacial phases during annealing at 200 ^{o}C at the interface vicinity. In Figure 5(c), a small change in the interface is observed with further out diffusion of In into Au/Cr layers. It is also noted that a small amount of phosphide (P) is out diffused into metal layers. This indicates the possibility of a P reaction with metal layers. These results lead to formation of phosphide (P) phases at interface during annealing at 300 ^{o}C as shown in Figure 5(c). Moreover, it is observed that a small amount of oxygen is observed in the interface for all contacts. This may be partially originated from the InP surface.





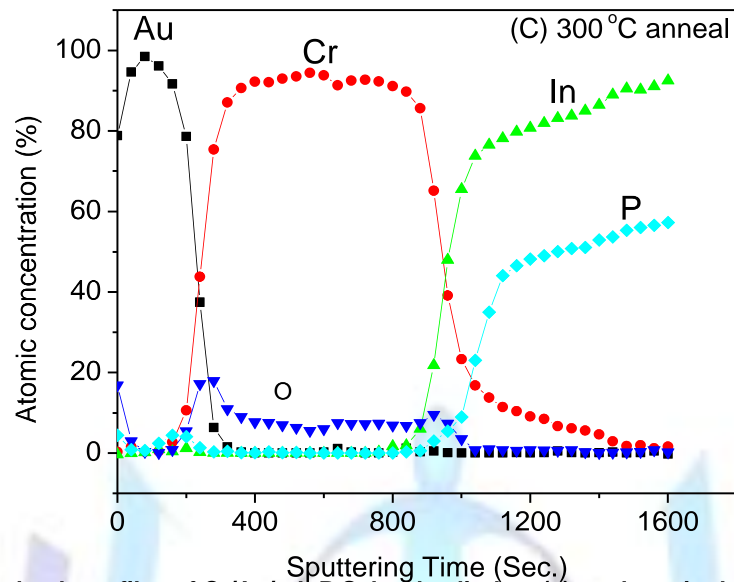
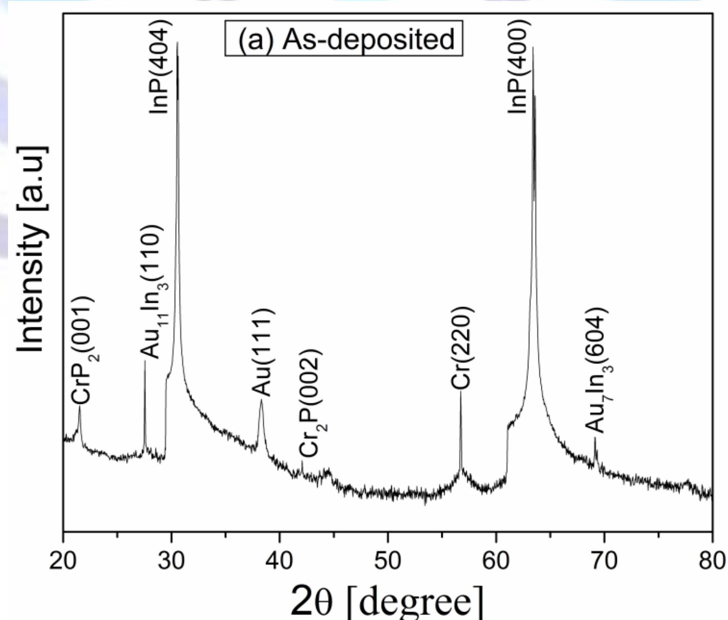


Figure 5. AES depth profiles of Cr/Au/n-InP Schottky diodes: (a) as-deposited, (b) 200 °C annealed and (c) 300 °C annealed contacts.

Next, In order to understand the interfacial reactions between deposited metal layers and semiconductor, XRD measurements are performed before and after annealing temperature. Figure 6 shows the XRD spectra of Au/Cr/ n-InP Schottky diodes at different annealing temperatures. For the XRD spectra of the as-deposited contact, Figure 6(a), in addition to the characteristic peaks InP (404), (400) and Au (111), Cr (220) there are some extra peaks which are identified as CrP_2 (001), $Au_{11}In_3$ (110), Cr_2P (002), Au_7In_3 (604). For the contact annealed at 200 ^{o}C (Figure 6(b)), additional peaks are observed compared to the as-deposited sample. This indicates the formation of new interfacial phases at the interface. These phases are identified as Au_3In (110), Au_3In (001), Au_9In_4 (211), Au_7In_3 (220), $CrIn_3$ (111), In_4Au_9 (321). Figure 6 (c) shows the XRD spectrum of the sample annealed at 300 ^{o}C. It is noted that the peaks corresponding to Au_3In (001), $CrIn_3$ (111) and In_4Au_9 (321) observed in the 200 ^{o}C annealed sample disappeared in 300 ^{o}C annealed sample. Further, a new peak is identified as CrP (102) compared to the as-deposited and 200 ^{o}C annealed sample (Figure 6(c)).



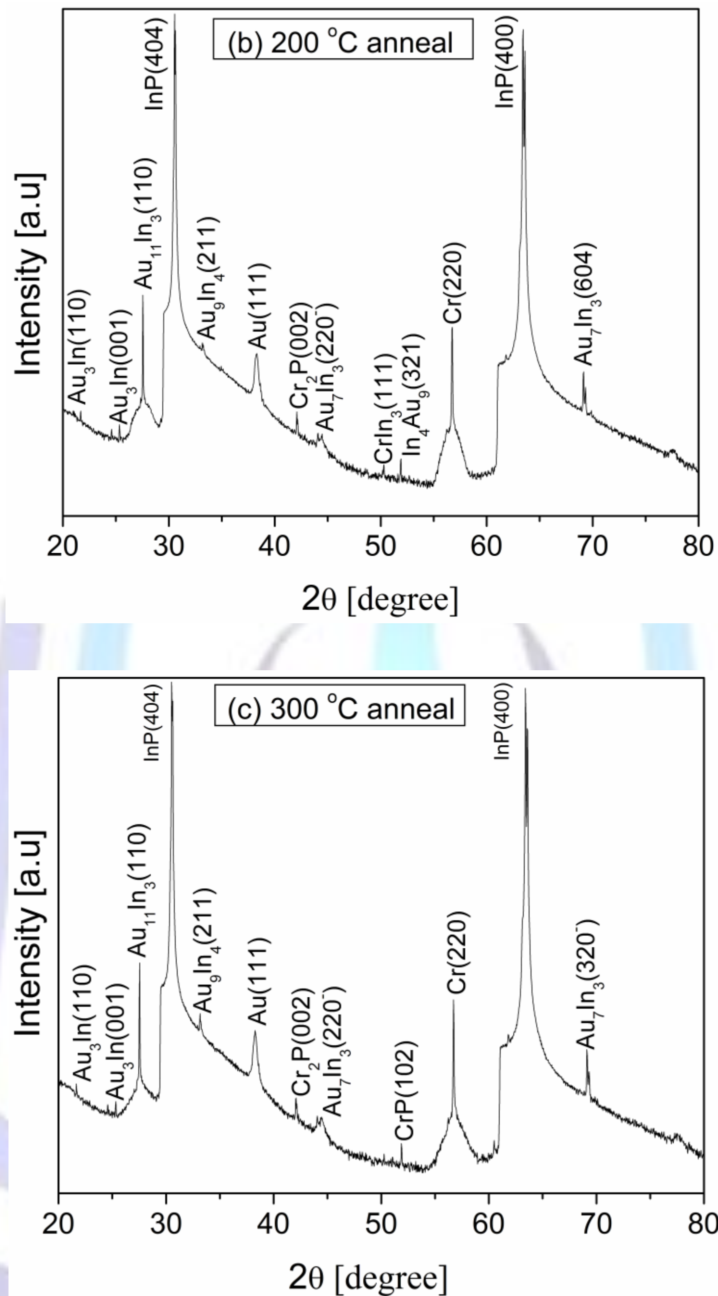


Figure 6. XRD plots of the Cr/Au/n-InP Schottky diodes: (a) as-deposited, (b) 200 °C annealed and (c) 300 °C annealed samples.

The atomic force microscopy (AFM) is also employed to characterize the surface morphology of the Au/Cr Schottky contacts before and after annealing at 300 °C in N_2 ambient for 1min. Figure 7 shows the AFM images of the as-deposited Au/Cr Schottky contact and annealed at 200 °C and 300 °C. The scanned area of the sample is 5×5 μm^2. The surface morphology of the as-deposited sample is fairly smooth with a root-mean-square (rms) roughness of 1.800 nm as shown in Figure 7(a). When contact is annealed at 200 °C, Figure 7(b), the surface morphology become somewhat degraded with an rms roughness of 3.075 nm. Further, increase in the annealing temperature up to 300 °C, Figure 7(c), it is observed that the surface morphology of the contact is slightly increased with an rms roughness of 7.307 nm as compared to the as-deposited and 200 °C annealed contacts. Results revealed that the Au/Cr Schottky contact has no change in surface degradation significantly even after annealing at 300 °C.

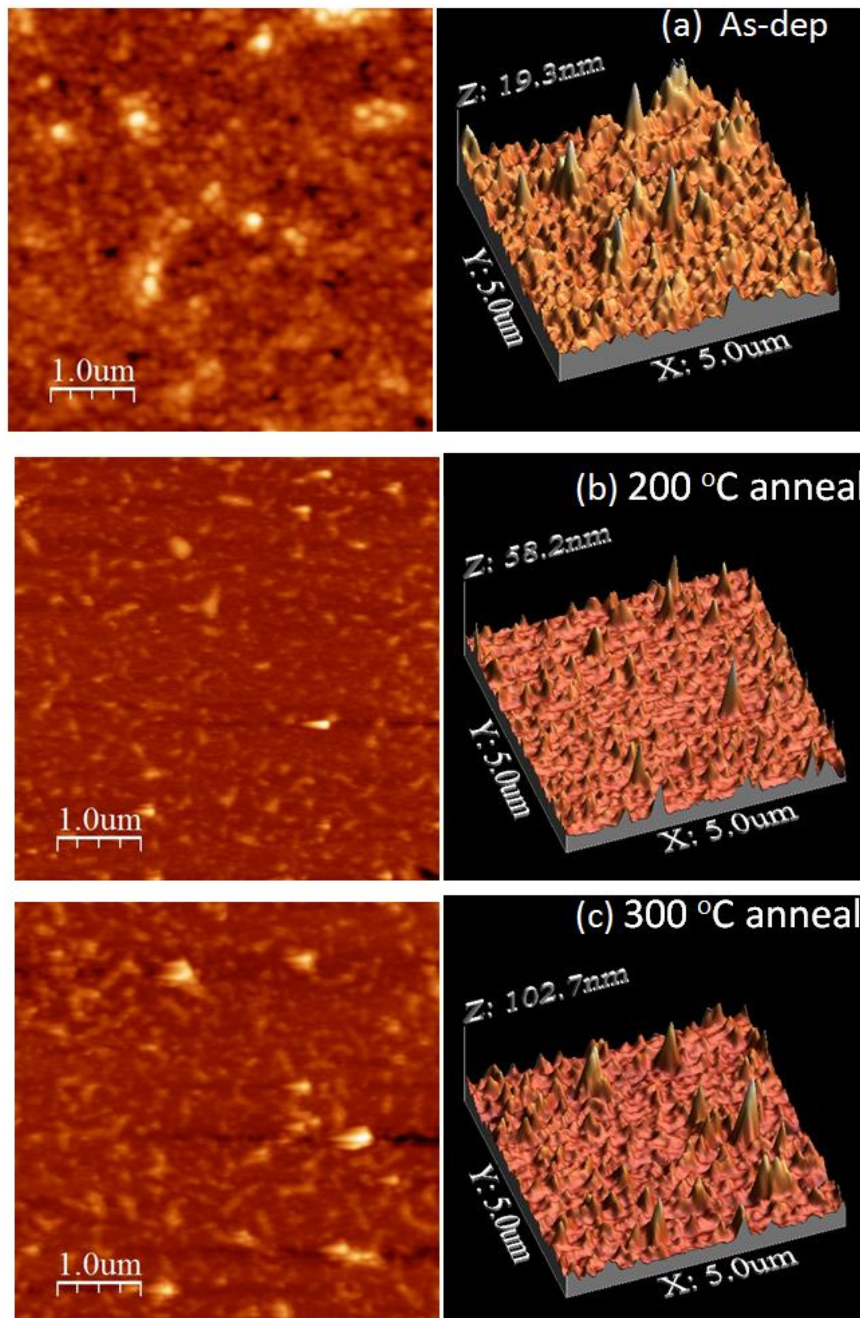


Figure 7. AFM micrographs of the Cr/Au/n-InP Schottky diodes: (a) as-deposited (b) 200 °C annealed and (c) 300 °C annealed samples.

The experimental results exhibit that the barrier height (BH) increases for the contact annealed at 200 ^{o}C compared to as-deposited and 100 ^{o}C annealed contacts. However, the BH slightly decreases in annealing temperature upto 300 ^{o}C. The variation in the BH on annealing may be responsible for the formation of interfacial phases at the interface. The variation in BH of Au/Cr/n-InP Schottky diodes with annealing temperature can be explained based on the AES and XRD results. The XRD and AES depth profile results reveal that, as annealing temperature increases up to 200 ^{o}C, an interfacial region formed at the interface, with the out diffusion of indium (In) from the InP into Au/Cr layers as evident from AES and XRD measurements (Figures.6 (b), 5 (b)). As a result, the formation of interfacial phases such as Au_3In (110) (001), Au_9In_4 (211), Au_7In_3 (220), $CrIn_3$ (111), In_4Au_9 (321) are responsible for the increase of the BH. The formation of these interfacial phases result in accumulation of fixed negative charge due to the presence of filled acceptors or electrons traps at the InP interface. The increase in the BH is always accompanied by a corresponding decrease in the reverse leakage current. However, the decrease in SBH upon annealing at 300 ^{o}C could be attributed the reaction of Cr layer with InP, resulting in the formation of phosphorous (P) phases at the interface vicinity (as evident from Figure 6(c)). The formation of phosphorous phases at interface may create phosphorus vacancies in InP which act as donors, as a result reducing the

SBH at elevated temperature. In this case a positive charge state may exist at the interface due to loss of phosphorous from the surface which may reduce the SBH. These findings are consistent with the results which were previously reported by Andersson [34], Naik et al. [14]. The discrepancy of the BHs of Au/Cr Schottky contacts is mostly due to the observed structural changes of the Au/Cr contacts at the interface.

4.CONCLUSIONS

The electrical, and structural properties of Au/Cr/n-InP Schottky diode have been investigated by I-V, C-V, AES and XRD measurements at different annealing temperatures. The estimated Schottky barrier height (SBH) and ideality factor (n) of the as-deposited Au/Cr/n-InP Schottky diode are 0.51 eV (I-V)/0.64 eV (C-V) and 1.81, respectively. When the contact is annealed at 200 ^{o}C in N_2 ambient for 1 min, a maximum SBH and low ideality factor are achieved for Au/Cr/n-InP Schottky diode and the corresponding values are 0.71 eV (I-V)/0.81 eV (C-V) and 1.15. However, the SBH slightly decreases to 0.58 eV (I-V)/0.69 eV (C-V), and ideality factor increases to 1.45 upon annealing at 300 ^{o}C. Further, it is noted that the SBHs extracted from the C–V measurements are higher than that obtained from I–V measurements. The SBHs obtained from the Norde and Cheung's methods are closely matched with those obtained from the I-V method. Results show that the optimum annealing temperature for the Au/Cr/n-InP Schottky diode is 200 °C. It is noted that the extracted interface state density N_{ss} decreases with an increase in annealing up to 200 ^{o}C and then slightly increases upon annealing at 300 ^{o}C. Based on the AES and XRD results, the formation of indium phases at the interface may be the reason for the increase of SBHs after annealing at 200°C. The decrease in SBH for contact annealed at 300°C may be the reason for the formation of phosphide phases at the interface. The AFM results show that the surface morphology of the as-deposited Au/Cr Schottky contacts (rms roughness of 1.800 nm) is increased for the contact annealed at 300 ^{o}C (rms roughness of 7.307 nm). Expermental results indicate that the Au/Cr Schottky contact may be good choice for the development of InP-based electronic device applications.

5.ACKNOWLEDGMENTS

The authors thank the University Grant Commission (UGC-SERO), Hyderabad for providing the financial assistance (No: F. MRP-4247/12 UGC-SERO dated: March, 2013).

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