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Reduction of the surface roughness of Ge-on-insulator layers up to sub-nanometer range by chemical mechanical polishing

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ABSTRACT

We are investigating the thermoelectric characteristics of Ge and SiGe nanostructures for realizing high power generator efficiency. In this paper, we investigated the influence of the thinning process on the surface roughness of a direct wafer-bonded p-type Ge-on-insulator (GOI) layer in order to realize an ultra-thin GOI substrate with extremely low surface roughness for the fabrication of Ge and SiGe nanostructures. The wafer thinning process was performed by chemical mechanical polishing (CMP) and wet chemical etching (WCE). A very smooth GOI layer with sub-nanometer (0.3 nm) surface roughness, suitable for nanostructure fabrication, was achieved using CMP compared to WCE process.

Indexing terms/Keywords

Ge on insulator, direct wafer bonding, chemical mechanical polishing, wet chemical etching.

Academic Discipline And Sub-Disciplines

Interdisciplinary physics

SUBJECT CLASSIFICATION

Nanoscale science, Materials Science

TYPE (METHOD/APPROACH)

High efficient nanostructured thermolectrics

INTRODUCTION

Nanostructured Ge and SiGe have attracted considerable attention for use in thermoelectric power generators to achieve a higher efficiency than that of Si devices[I-IV]. To fabricate Ge and SiGe nanostructures by photolithography, ultra-thin Ge- and SiGe-on-insulator (GOI and SGOI) substrates with extremely low surface roughness are required[V]. Despite tremendous efforts made by researchers, preparation of ultra-thin GOI and SGOI substrates with sub-nanometer surface roughness remains a challenging task[VI,VII]. Moreover, there are several issues to be resolved regarding the properties of ultra-thin GOI and SGOI substrates. One of the issues that arise during the fabrication process, such as direct wafer-bonding is surface roughening during annealing, which usually performed to further enhance the bonding strength of GOI and the other is crystallinity degradation in the GOI and SGOI layers. From the viewpoint of size effect in nanostructures, surface roughness degrades the quantum effect owing to the fluctuation in quantized energy states. The electronic properties of the nanostructured Ge and SiGe are also degraded by the increase in carrier scattering resulting from the higher surface roughness and defect formation. Hence, the surface roughness must be reduced up to the sub-nanometer range.

In the current state of the art of Si-based electronic devices, the minimum feature size is now less than 10 nm in dimension. This is possible because the electronic device grade of Si surface roughness is below 0.2 nm[VIII,IX], which can be achieved through chemical mechanical polishing (CMP). However, in the case of Ge, it is too difficult to achieve such a low surface roughness on a direct wafer-bonded GOI surface without damaging the interfaces of the device. Moreover, a series of annealing and pressing process must be performed and a thin intentionally grown thermal oxide layer is needed to reduce the surface/sidewall roughness of the GOI[X-XII]. Therefore, reducing the surface roughness of a direct wafer-bonded GOI substrate remains a challenging matter.

In this paper, we describe the investigation of two different thinning processes, used to obtain GOI layers with minimal surface roughness. The root-mean-square (RMS) roughness values of direct wafer-bonded GOI surfaces thinned by either CMP or wet chemical etching (WCE) were comparatively analyzed in pursuit of an extremely flat GOI surface with sub-nanometer roughness for the fabrication of Ge nanostructures. Moreover, the obtained RMS roughness was relatively low compared to previously reported values.

EXPERIMENTAL METHODS

A 300-μm-thick p-type Ge(100) wafer and a 370-μm-thick thermally-oxidized p-type Si wafer with an oxide thickness of 100 nm were used for the fabrication of a GOI substrate by direct wafer-bonding. After bonding, the GOI substrate was

subjected to a thermal annealing treatment at 400 °C in an N_2 atmosphere for 1 h to further strengthen the bonding at the Ge/SiO_2. Subsequently, thinning was performed by mechanical polishing with slurry containing diamond particles[XIII], to reduce the GOI layer thickness to below 5 µm. The samples were then divided into two groups. The first group was polished by mechanical polishing (MP) combined with CMP using colloidal silica (Glanzox 3000) with the polishing rate of 10 µm/min. The second group was polished by mechanical polishing combined with WCE in an H_3PO_4:H_2O_2:H_2O solution, at an etch rate of 130 nm/min[XIV]. The CMP and WCE thinning processes of GOI layer were performed in the room temperature at around 24 °C. The thinning process tools for MP combined with CMP and WCE were shown in Figures 1(a and 1(b). Table. 1 shows the thinning process conditions for obtaining sub-nanometer surface roughness in direct wafer-bonded GOI layers.

The surface morphology of the thinned GOI layers was observed by dynamic force microscopy (DFM), with scanned areas of 2 µm x 2 µm and 10 µm x 10 µm. RMS roughness values were determined from the DFM images. The GOI layer thickness and the quality of the Ge/SiO_2 interface were characterized by scanning electron microscopy (SEM). Optical microscopy was used to observe the formation of etch pits and hillocks on the GOI surface over a larger area.

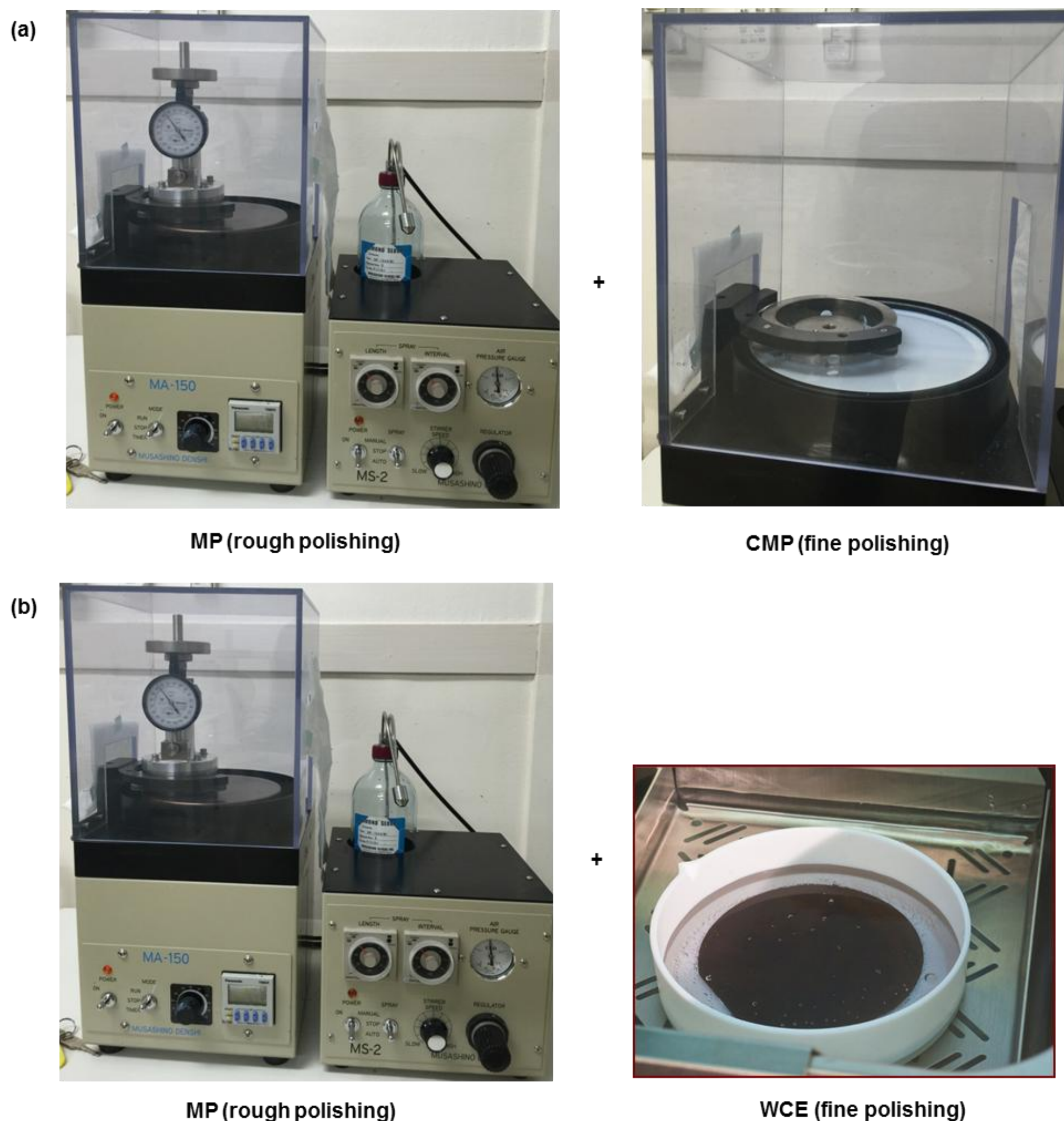

Fig 1: Thinning process tools (a) MP combined with CMP and (b) MP combined with WCE.

Table 1. Thinning process information of p-type Ge-on-insulator layer.

Thinning type	Mechanical polishing (rough)	Chemical mechanical polishing (fine)	Wet chemical etching process
Material	Diamond slurry	Colloidal silica slurry	H_2O_2+H_3PO_4+H_2O (1:6:3)
Slurry partical size	3μm	0.06~0.08μm	
pH	9.8	10.8	
Condition	Room temperature	Room temperature	Room temperature
Polishing rate	10μm/min	1μm/h	130nm/min

RESULTS AND DISCUSSIONS

Figure 2(a) shows a DFM image of an as-prepared GOI surface after the thermal annealing process. The RMS roughness of the surface was approximately 27.0 nm. Figures 2(b) and 2(d) show 2 μm x 2 μm scanned DFM images of GOI surfaces after CMP and WCE processes, respectively. GOI layers thinned by CMP and WCE had RMS roughness values of 0.3 and 0.9 nm, respectively. Furthermore, the sub-nanometer roughness values remained 0.4 and 1.0 nm even over the 10 μm x 10 μm scanned area, as shown in Figures. 2(c) and 2(e). These observations indicate that the CMP process has great ability in realizing sub-nanometer roughness and leads to a smoother surface than the WCE process. The SEM images in Figures. 3(a) and 3(b) show the resulting layered structure of GOI substrates consisting of top Ge, buried oxide (BOX) layer and bottom Si substrate, thinned by CMP and WCE, respectively. The layer thickness of the top Ge layers thinned by CMP and WCE are 189 and 334 nm, respectively. The SEM image of the GOI substrate thinned by CMP shows a very flat interface between the GOI and BOX layers. Therefore, in the fabrication of ultra-thin electronic grade GOI substrates through a direct wafer-bonding technique, CMP is preferable to WCE without damage to the other components in the device. The crystallographic analysis of the Ge/SiO_2 interface remains unclear and a more detailed analysis is highly desirable.

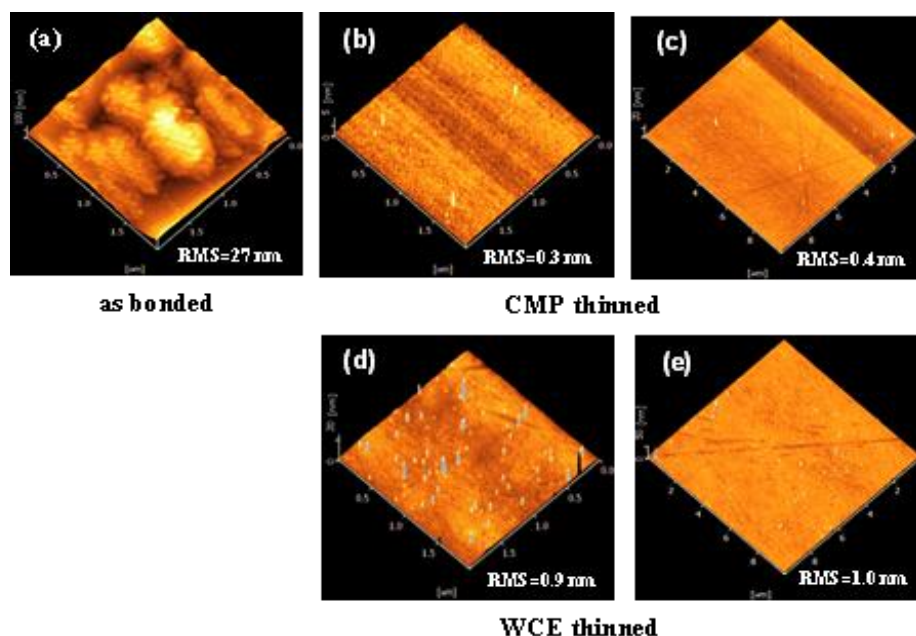

Fig 2: DFM images of (a) as bonded, (b),(c) CMP-thinned, and (d),(e) WCE-thinned GOI layers.

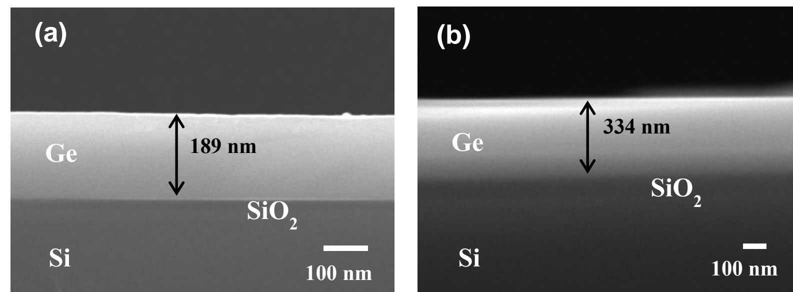

Fig 3: Cross-sectional SEM images of (a) CMP-thinned and (b) WCE-thinned GOI substrates.

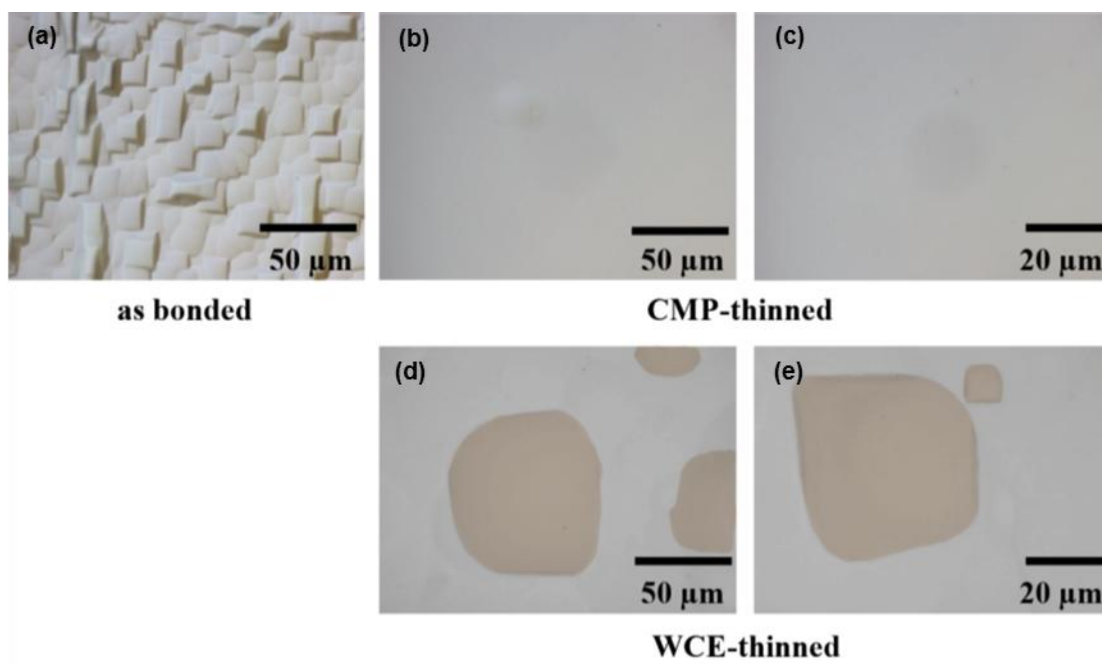

Fig 4: Optical photographs of (a) as bonded, (b),(c) CMP-thinned, and (d),(e) WCE-thinned GOI layers.

In order to observe defect formation over a larger area, the surfaces of as-bonded and thinned GOI layers were investigated. In the WCE process, the etching solutions are usually sensitive to the local stress level, so the etch rate of the perfect crystal lattice differs from the etch rate at defect sites[XV]. This anisotropic etching creates etch pits or hillocks, which can be identified and counted using a digital optical microscope. Figures 4(a), 4(b) and 4(c) show optical photographs of the surfaces of as-bonded and CMP-thinned GOI layers. The figures clearly show that no development of etch pits was observed after mechanical polishing combined with CMP. However, etch artifacts were identified on the surface of the GOI layer after WCE processing. The irregular square-shaped defects shown in Figures. 4(d) and 4(e) are clearly ascribed to etch artifacts. They do not all have the same crystal defect because their shapes, sizes and edges differ from those of a regular etch pit pattern and their orientation is non-crystallographic in nature. Furthermore, the squares were too large to be related to crystal defects. Therefore, the formation of the etch artifacts was not related to crystal defects nor was it an anisotropic etching effect. The etch artifacts are probably due to the chemical precipitation of excess phosphorus ions present from the etching solutions.

As a result, a very smooth device grade GOI layer can be achieved through CMP rather than WCE. Therefore, we believe that, GOI layer thinned by CMP process is essential for the enhancement in the electronic properties of future nanostructured Ge-based thermoelectric devices.

SUMMARY

We fabricated a p-type GOI layer using a direct wafer-bonding technique and confirmed that the GOI surface was rough after the annealing process. We analyzed the influence of the layer thinning process on the surface roughness of the GOI layer and obtained a device grade GOI surface with an RMS roughness of ~0.3 nm by mechanical polishing combined with CMP. Furthermore, optical and SEM images showed a high interface and crystal quality in the CMP-thinned GOI substrates, which should make them suitable for the fabrication of ultra-thin GOI surfaces through direct wafer-bonding for future advanced Ge and SiGe nanostructures.

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