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RECONFIGURABLE LOW POWER AND AREA EFFICIENT ESPFFIR FILTER USING VHBCSE MULTIPLIER

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ABSTRACT

Reconfigurable Even Symmetric Parallel Fast Finite Impulse Response (RESPFFIR) filter shall be utilized as the Processing Element (PE) in Software Defined Radio (SDR) design to improve the throughput. The number of multipliers required in RESPFFIR filter increases when parallelism length increases. The Constant Multiplier (CM) technique is used to diminish the power consumption in FIR filters by reducing the number of Logical Operators (LO) and Logical Depth (LD). Binary Common Subexpression Elimination (BCSE) method is suitable to exploit symmetric coefficient in FIR filters. The Vertical Horizontal Binary Common Subexpression Elimination (VHBCSE) technique based Constant Multiplier (CM) design further diminish the number of LO and LD. The 2-bit BCSE algorithm has been applied vertically across neighboring coefficients and HCSE makes use of CSs that arise within each coefficient to eradicate redundant computations, which intern reduce logical operator in constant multiplier. This paper presents the design of Reconfigurable Even Symmetric Parallel Fast Finite Impulse Response (RESPFFIR) filter using VHBCSE based CM multiplier, which is reconfigurable with reduced power and area consumption without degrading the throughput. The power consumption reduces by 12% and the area required gets reduced by 24% in the proposed design when compared with existing CSE Hcub-n Multiple Constant Multiplier based ESPFFIR filter design. The analysis is done using Cadence RC synthesize tools.

Keywords

ESPFFIR - Even Symmetric Parallel Fast Finite Impulse Response, CS - Common Subexpression, Hub - Heuristic of cumulative benefit, BCSE-Binary Common Subexpression Elimination, VHBCSE - Vertical Horizontal Binary Common Subexpression Elimination.

Academic Discipline And Sub-Disciplines

Information and Communication Engineering , VLSI Signal Processing

SUBJECT CLASSIFICATION

Parallel FIR filter design.

TYPE (METHOD/APPROACH)

Vertical Horizontal Binary Common Subexpression Elimination (VHBCSE).

1. INTRODUCTION

The requirement for high-performance and low-power Digital Signal Processing (DSP) systems is getting higher and higher. Finite-impulse response (FIR) digital filters are the most extensively used essential device in DSP systems, ranging from communications to audio, video processing and in Multiple Input Multiple Output (MIMO) systems. In MIMO system parallel processing enhance the sampling rate by replicating hardware so that many inputs can be evaluated in parallel and several outputs are produced at the same time, at the disbursement of increased area and power consumption. Number of multiplier used in the parallel FIR increases when the number of subfilter used in the filter structure increases. The parallel FIR filter configuration based on Fast Finite Impulse Response (FIR) Algorithms (FFAs) restrain the usefulness of polyphase decompositions, which can decrease the number of multiplications in the subfilter module by utilizing the symmetric coefficients property for designing ESPFFIR filter structure[12][13]. The remarkable applicability of ESPFFIR filter stimulate the system developer to design the FIR cores with lower power and low area along with the ability to function with high throughput. In any fast parallel FIR filter, the multipliers are the major datapath elements which intensify the area and power consumption of the desired filter. The Common Subexpression Elimination (CSE) schemes based on Canonical Signed Digit (CSD) coefficients generate low complication in FIR filter coefficient multipliers [10][3]. The purpose of CSE is to classify multiple incidences of the same bit patterns that are occurred in the CSD representation of coefficients, and eradicate these redundant multiplications. A 2-bitCSE method categorizes the suitable patterns for the eradication of redundant computations and optimization [10] [12]. In [4], the method in [14] was modified to reduce the logic depth (LD) and speed up the calculation. In [2], the Binary Common Subexpression

Elimination (BCSE) technique was used to enhance the adder diminution for low complexity FIR filters design. The Common Subexpression Elimination (CSE) method reduces the logic operators and logic depth to realize ESPFFIR filters with low complexity. Two classes of common subexpressions occur in filter coefficients are the horizontal and the vertical subexpressions [11][8]. In VHBCSE algorithm the horizontal and the vertical elimination technique reduces the logic depth and logic operators. The competence in terms of speed, power and area of the constant multiplier has been improved while designing a reconfigurable FIR filter by preferring 2-bit long BCS obviously[5]. To design an efficient RESPFFIR filter, the VHBCSE algorithm based on the 2-bit BCSE is applied vertically across neighboring coefficients and horizontally within the coefficient.

In this paper, the Even Symmetric Parallel Fast Finite Impulse Response (ESPFFIR)filter is designed using VHBCSE based CM to consume less power and to occupy less area compared with Heuristic of cumulative benefit (Hcub) based ESPFFIR filter. This paper is structured as follows. In Section 2, the ESPFFIR filter structures are presented. In Section 3, VHBCSE based sub-filter design is discussed. Section 4 presents VHBCSE based RESPFFIR filter design. In Section 5 Conclusion.

2. ESPFFIR FILTER STRUCTURE

In L-parallel, 24-tap (N) filter , let the coefficients be

$$\{h(0), h(1), h(2), h(3), h(4).....h(N-1)\}$$

If they are symmetric, that is

$$h(n) = h(n+N-1)$$

The subfilters are as follows

$$H_0 = \sum_{n=0}^{10} h(2n)$$

$$H_1 = \sum_{n=0}^{10} h(2n+1)$$

$$H_0 + H_1 = \sum_{n=0}^{10} h(2n) + h(2n+2).....(1)$$

Using the symmetry of the coefficients, the structures are shown in Fig.1. and Fig.2. In 2-parallel ESPFFIR filter there are 12 multipliers for the subfilter H_1.Each subfilters ($H_0 + H_1$) and ($H_0 – H_1$) have 6 multipliers, totally 24 multiplier for the filter structure.

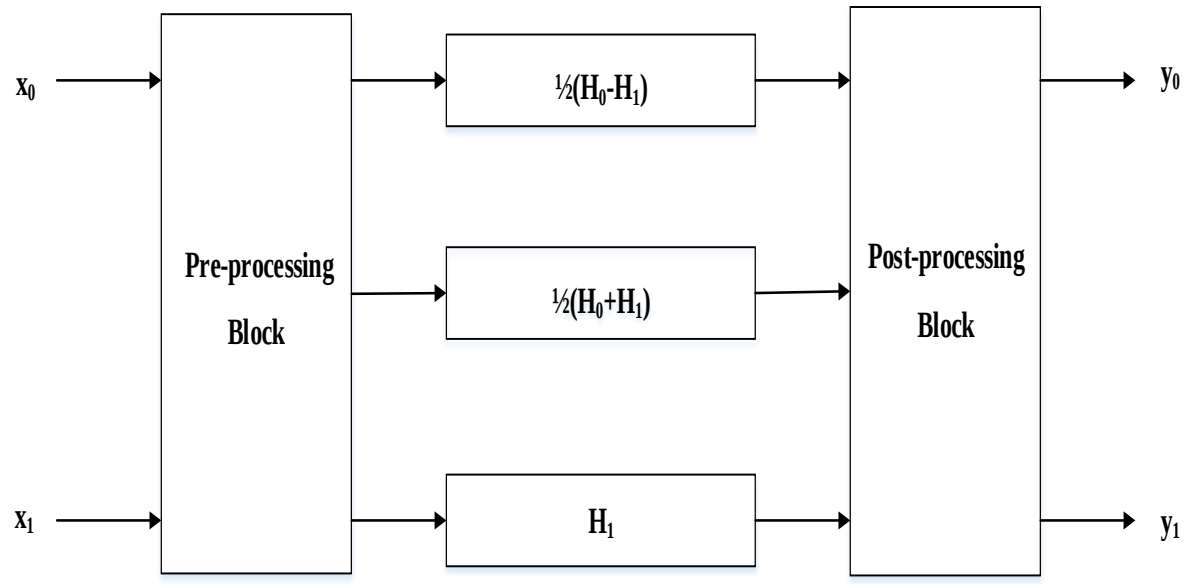

Fig 1: 2- Parallel ESPFFIR filter

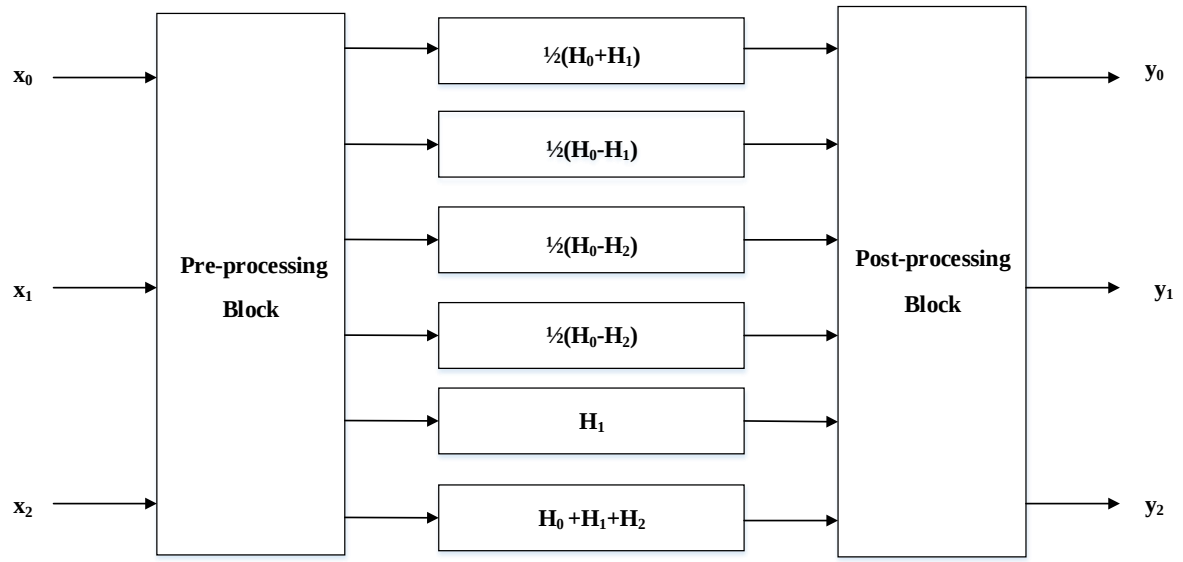

Fig. 2: 3- Parallel ESPFFIR filter

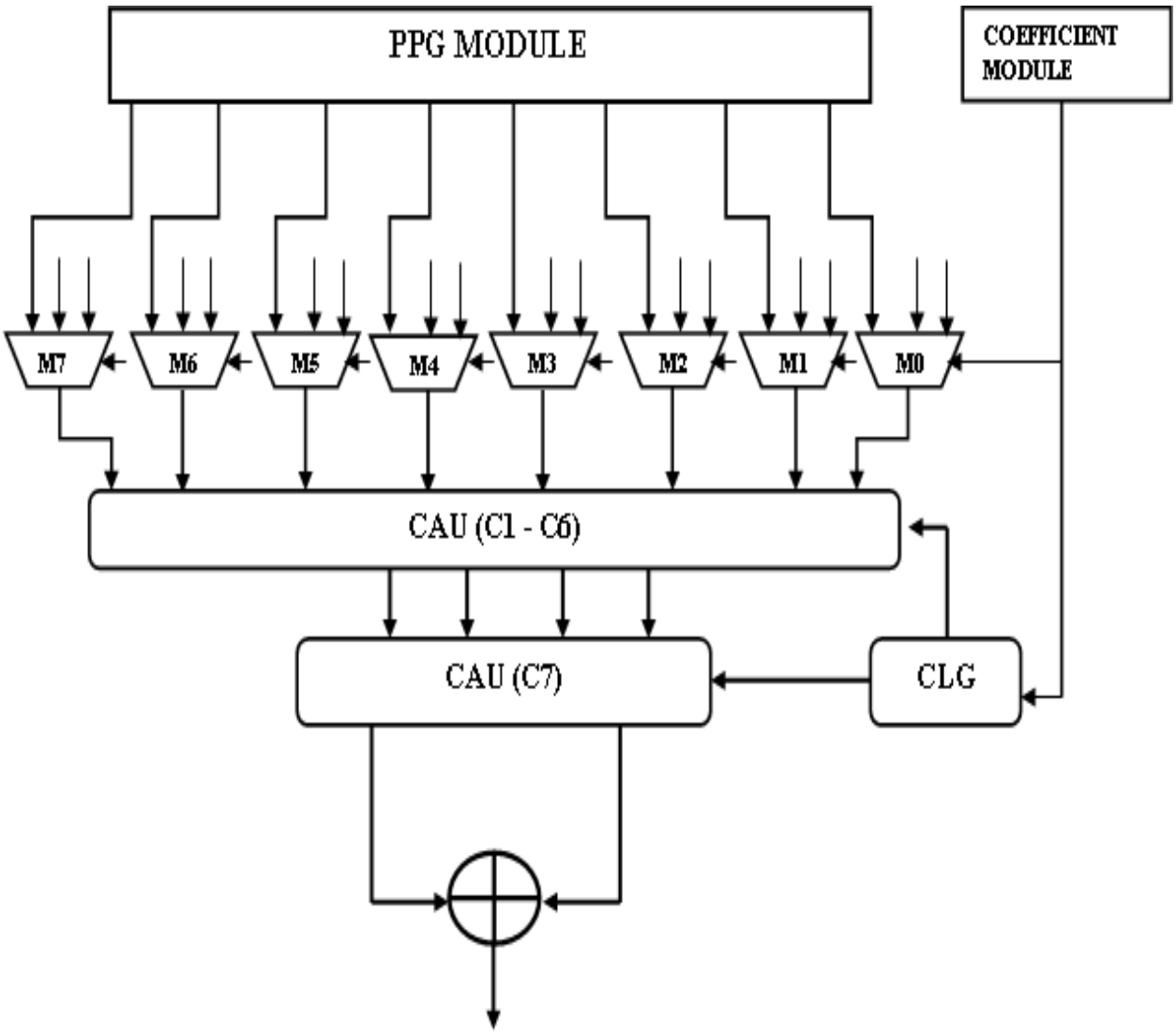

Fig. 3: VHBCSE based Reconfigurable constant multiplier architecture

Table I

2-bit and 4-bit VBCSE and HBCSE

H(15)	H(14)	H(13)	H(12)	H(11)	H(10)	H(9)	H(8)	H(7)	H(6)	H(5)	H(4)	H(3)	H(2)	H(1)	H(0)
1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	0
1	1	1	0	1	1	1	1	1	1	0	1	0	1	1	1
1	1	1	1	1	0	1	1	1	1	0	1	0	1	0	1

The 3-parallel Filter structure is shown in Fig. 2. Here the subfilters H_1 and $H_0 + H_1 + H_2$ are symmetric and they require 4 multipliers each and the remaining four subfilters have 8 multipliers each, which intern of 32 multipliers for the filter structure [12].Still the parallel filters have a large number of multipliers and adders which increase with the area and power consumption. Constant Multipliers (CM) technique utilizes the redundancy in the expression to diminish the Logical Operators (LO) and Logical Depth (LD). Various CSE based algorithms like Heuristic of cumulative benefit (Hcub), n-dimensional Reduced Adder Graph (RAG-n) and Bull Horrocks Modified algorithm (BHM) are analyzed for designing Multiple Constant Multipliers in ESPFFIR filter in [9].While the above algorithms are used for the design of Multiple Constant Multipliers, the CSE- Hcub-n use 40% less number of adders than CSD based SCM multipliers. It is understood that the CSE-Hcub-n algorithm is superior to other algorithms in designing the sub-filters in the ESPFFIR filter [9].The Binary Common Sub-expression Elimination (BCSE) scheme sinking the number of adders for designing multiple constant multipliers. The horizontal and the vertical elimination techniques are used to reduce the logical depth and operators in VHBCSE algorithm. The competence in terms of speed, power, and area of the constant multiplier has been improved in the work offered in [9] while designing a reconfigurable ESPFFIR filter by preferring 2-bit long BCS observably [5].

3. VHBCSE BASED SUBFILTER DESIGN

VHBCSE is used for eradicating the BCSs present within the coefficient and the adjutant coefficients respectively. Let us take into account a reconfigurable multiplier with 16-bit input (X) and the coefficient (H) with same bit width. The multiplication using shift and add operation between the inputs(X) with the coefficient value of all 1's has been written as below

$$X * H = \sum_{k=1}^{16} x^{-k} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

In VHBCSE method a 2-bit VBCSE is applied on the nearby coefficient and the 4-bit, 8-bit HBCSEs are used to detect and eradicate as many BCSs present within each coefficient. The 2-bit CSE can be written as

$$x_1 = x + x^{-1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Substituting (3) in (2)

$$X * H = \sum_{k=0}^{7} x_1^{-(2k+1)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

The expanded form of equation (1) generates eight partial products and these are added by the Multiplier Adder Tree (MAT). Fig. 3 shows the architecture of the VHBCSE based subfilter [5] for RESPFFIR filter design. Fig. 4 shows the data flow representation of the VHBCSE algorthim. A register is used to store the sampled inputs and the coefficients are stored in the Look Up Tables. The different blocks of VHBCSE based CM multiplier are Sign Conversion Unit, Partial Product Generator (PPG) module, Control Logic Generator (CLG), Multiplexers Unit and Controlled Addition Units. Sign conversion Unit is used for the signed decimal value representation for the input and the coefficient. The Partial Product Generator (PPG) modules shift and add operations is used to generate the partial product output. These partial products are summed to generate multiplied output. Multiplexer's are used to select the appropriate partial product depending on the coefficient value. Control Logic Generator (CLG) module take multiplexed output as input and group them into 4-bits and 8-bits, generate 7 control signals. In the Controlled Addition units A1-A4 and AS1-AS6 adders are controlled depending on the control signals C1-C7 to produce the added output. An example for 2-bit and 4-bit VBCSE and HBCSE is shown in the Table I.

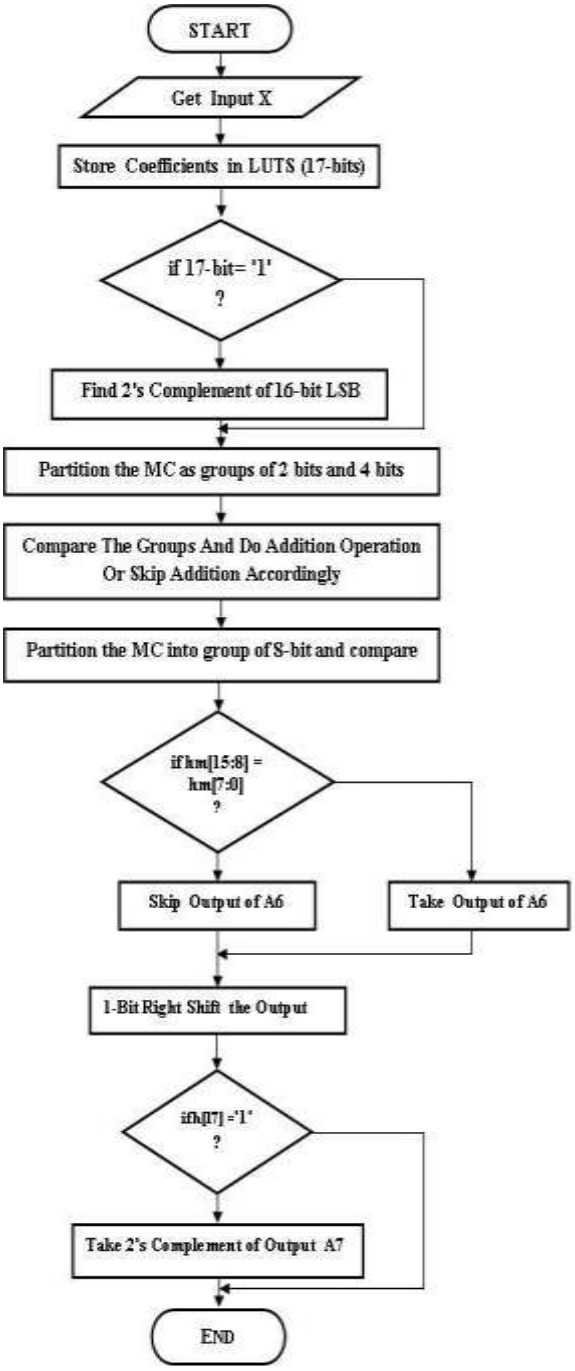

Fig. 4: Data flow representation

4. PROPOSED VHBCSE BASED RESPFFIR FILTER DESIGN

The VHBCSE based 2-parallel RESPFFIR is shown in the Fig.5. The Subfilter block (H_0-H_1), (H_0+H_1) and the H_1 of the existing ESPFFIR filters are replaced by VHBCSE based reconfigurable coefficient based subfilters. The pre_processing and post_processing block of RESPFFIR block is designed by using Modified CLSA adder as in [7], [9]which consume less power and area. The existing reconfigurable FIR filter in [4],[2],[5],[6] are transposed form **Table II**

Performance Comparison of Area, Power and Delay

Method	Area(mm^2)	Power(nW)	Delay(ps)
VHBCSE	10056	864056	6807
Hub- n	34044	2071973	13250

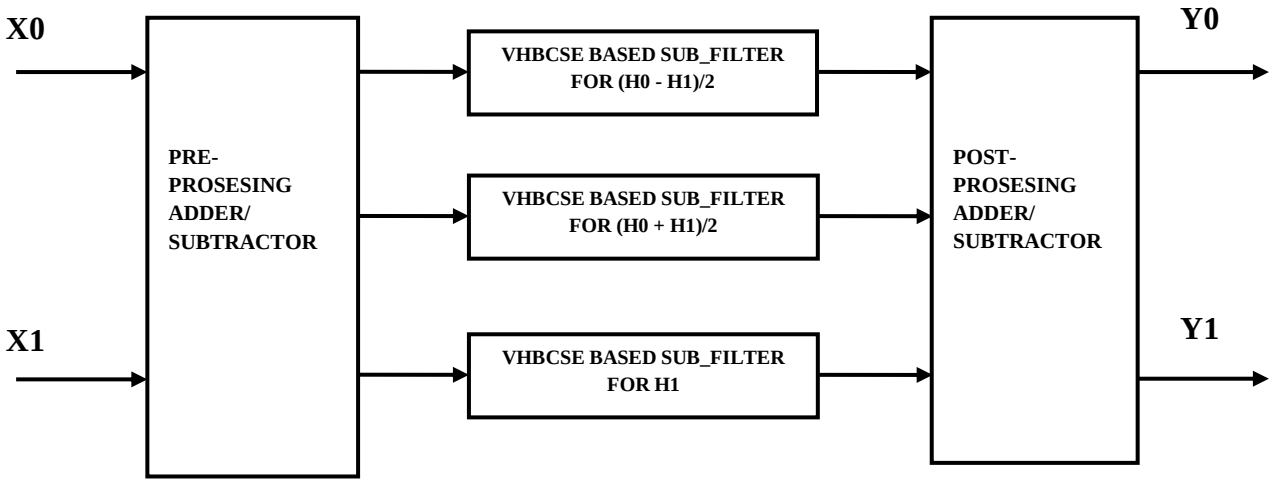

Fig. 5: VHBCSE based 2-parallel RESPFFIR filter

non parallel FIR filters with low throughput. The proposed VHBCSE based RESPFFIR filter is designed to consume low power with less area utilization and high throughput. As mention in [12],[13] the symmetric coefficient property deduces the number of multipliers used in the parallel FIR design with small overhead of adders used the pre-processing and post-processing module. Normally the parallel filters consume more area due to their hardware replication and the multipliers in the subfilters are more power hunger and area consuming datapath element. So, in this proposed reconfigurable parallel filter multipliers are designed by 2-bit BCSE algorithm by applying vertically across neighboring coefficients and HCSE make use of CSs that arise within each coefficient to eradicate redundant computations, which in turn reduce logical operator used for designing the constant multiplier. A VHBCSE based 2-parallel RESPFFIR filter was designed and their area, power and delay are compared with CSE Hcub-n Multiple Constant Multiplier based ESPFFIR filter. The comparison chart is shown in Fig. 6.

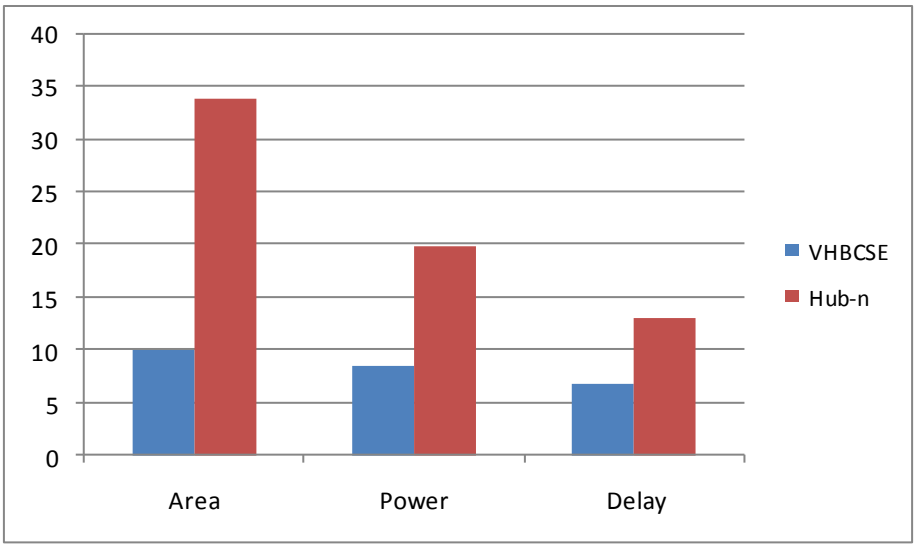

Fig. 6: Comparison of area, power and delay

5. CONCLUSION

This paper proposes the resourceful design of Reconfigurable Even Symmetric Parallel Fast Finite Impulse Response (RESPFFIR) filter for high throughput with low power and low area consumption. The high throughput is obtained by parallel FIR filter structure and the symmetric property of the coefficients reduces the number of multipliers needed for the parallel filter by considerable level. The multipliers' power consumption and area utilization is reduced by using VHBCSE technique used in subfilters of RESPFFIR filter. The VHBCSE subfilters are designed by 2-bit BCSE algorithm, which applied vertically across neighbouring coefficients and HCSE make use of CSs that arise within each coefficient to

eradicate redundant computations, which in turn reduce logical operator used for designing the constant multiplier. The proposed design consume 12% less power and 24% less area compared with the conventional design of CSE Hcub-n Multiple Constant Multiplier based ESPFFIR filter design.

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