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EXPERIMENTAL INVESTIGATION ON CASCADED MULTILEVEL INVERTER USING SINGLE VOLTAGE SOURCE TOPOLOGY

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ABSTRACT

This paper presents a cascaded H-bridge multilevel inverter with single DC source. Generally, each phase of the multilevel inverter requires 'n' number of DC sources for 2n+1 level. In this paper we have proposed a multilevel topology which requires only one DC source for all the three phases and other sources are replaced by ultra capacitors. Initially, the performance of multi level inverter has been studied by including all DC sources. Finally a single DC source is allowed and remaining n-1 DC sources are replaced by ultra capacitors. An adaptive PI controller is introduced for automatically maintaining the voltage level of capacitor and we use higher number of output levels to increase the quality of power. Comparison between both the cascaded multilevel inverter using DC source and ultracapacitor as source has been studied and it shows that the overall performance of ultracapacitor source is better than that of DC source. An experiment has been performed and the result shows that the proposed system is suitable for medium power applications.

Indexing terms/Keywords

cascaded multilevel inverter, DC source, H-bridge, ultracapacitor, adaptive voltage control.

Academic Discipline And Sub-Disciplines

Electrical and Electronics Engineering, Power Electronics and drives ;

SUBJECT CLASSIFICATION

Power Electronics

TYPE (METHOD/APPROACH)

Experimental setup and output was verified.

I. INTRODUCTION

Multilevel inverters are more familiar in industries for high power applications. A new topology for sub multilevel inverter has been studied by Mohammed et al [1]. This method utilizes less number of DC voltage sources, switches, and standing voltage on the switches that are analyzed by symmetric and asymmetric cases. Multi level inverters are used in motor drivers of EVs. The benefits and control scheme of cascaded multi level inverter has been analyzed. A new control method for stabilizing the voltage of multilevel inverter is tested under various conditions. It consists of single phase full bridge unit for all the phases and it produces an output waveform of 11-levels [2]. Multilevel inverters has low frequency ripple and it is transferred to the load, produces undesirable distortion in the voltage and current. A simple feed forward method has been introduced to avoid the ripple for carrier based modulation. The system automatically tracks the fundamental components and rejects the ripple harmonics [3]. A support vector machine and fuzzy based harmonic elimination method is introduced for multi level inverter. The distortion can also be eliminated by changing the switching angle and the frequency input given to the inverter [4]. A new topological method for 500HP induction machine with multi level inverter has been proposed by Madhav and Thomas [5].

Different design parameters such as capacitor voltage balancing, spectral structure have been discussed. Comparative study of symmetric and anti symmetric, seven level H-bridge inverter for induction motor for lower switching losses and output voltage optimization. In this comparison, asymmetrical structure provided the output very close to sinusoidal with very low distortion and less switching devices [6]. A multilevel inverter with less number of switches is used for driving motor and it allows operating in regenerative mode. A new control scheme is introduced for balancing the capacitor voltage without any phase shift and the input harmonics which also can be eliminated [7]. Topologies used in multilevel inverters are important in high power control applications. Three different topologies with various modulation techniques have been discussed by Jose et al [8]. Renewable energy utilization becomes popular and power electronics is required for interfacing source to the grid. Cascaded multilevel inverters are widely used to interface different renewable sources. A dual buck topology was used in the multilevel inverter along with control algorithm is introduced for reducing the ripple current [9]. Multilevel inverters with more voltage levels will provide high quality output.

A single multi voltage source is introduced to achieve more number of levels and less number of switches. A comparison study was performed between conventional topology and the single source topology [10]. Multilevel inverters require individual DC source for a cell. A new control algorithm with phase shift modulation is used in the cascaded H-bridge for

good voltage regulation [11]. A cascaded H-bridge inverter is introduced for an electric vehicle with direct torque control scheme was studied by Farid Khoucha [12]. This system produces almost sinusoidal output with very less distortion. Asymmetrical multilevel inverters are optimized and require more number of independent power sources. A new high frequency link was introduced for 27-level asymmetric inverter which had been studied by Juan et al [13]. This scheme reduces the number of voltage source by one. A general method of generating space vector pulse width modulation for multilevel inverter has been studied and it can be extended for n-levels [14]. A generalized algorithm has been developed for controlling the switching functions of the multilevel inverter. Comparison of different parameters of both the battery and ultracapacitor (ucap) are shown in Table 1. The remainder of this paper is organized as follows: section 2 describes the overview of proposed system; section 3 describes the proposed single DC source topology; section 4 explains the simulation results; and finally, conclusion is discussed in section 5.

II. SYSTEM DESCRIPTION

The master switches (MS) and the two stage H-bridges for each phase denoted by H_{R1}, H_{Y1}, H_{B1} and H_{R2}, H_{Y2}, H_{B2} are interfaced with the ucap module. It has various capacitance values which contains different racks. The power supplies required for a 27 level inverter using this topology is 7, which can be replaced by only one with the help of ucap module. Each phase of the multilevel inverter is interfaced with the ucap module and the output of H-bridge is connected to the induction motor (IM) is shown in Fig. 1.

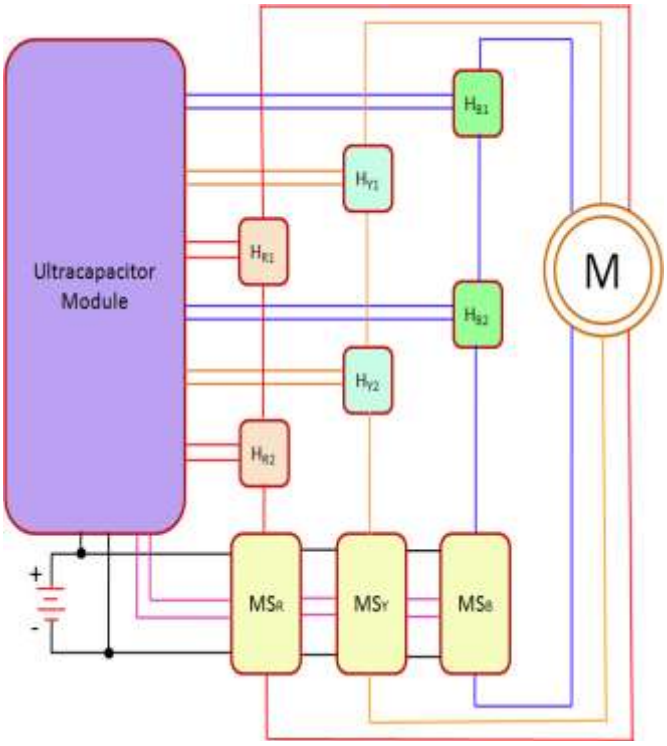

Figure 1. Proposed single DC source topology

The switch MS_R is in series with the two H-bridges H_{R1}, and H_{R2} with respect to R-phase. The suffix R, Y, B indicates each phase of the inverter and H1, H2 represents the first and second H-bridge respectively.

The three main switches MS_R, MS_Y, and MS_B are connected in parallel to the single DC source. The source voltage of MS_R, H_{R1}, H_{R2} can be adjusted in such a way that the ratio 6:2:1 should be maintained in the DC link voltage of R-phase (line-to-neutral) for avoiding additional voltage distortion. The gate signal is generated with the help of triangular carrier wave and compared with the reference signal. Both the frequency and magnitude of the sinusoidal pulse width modulation (SPWM) depend on the frequency and magnitude of triangular carrier wave. For n-level inverter, we require (n-1) level shifts of carrier for comparing the 3-phase reference signals [16] and [17].

The novelty of the proposed multilevel inverter is:

- The number of DC sources will be reduced.
- The proposed inverter structure produces more voltage levels and less THD.
- Coupling transformers are not necessary.
- Ultra capacitors are used so that extra filters are not necessary and the output waveform also has less distortion.

In this study, we are measuring different parameters for one phase (R-phase) for simplicity and it assumes that the parameters are equal for other phases.

III. CASCADED TOPOLOGY WITH ULTRACAPACITOR

Reduction of voltage source is required in cascaded multilevel inverters particularly when used in EVs. The combinational topologies have more advantages than the fundamental topologies. The power quality depends on the number of levels used. In this work we have proposed single DC source topology combined with ucap module as a source.

3.1. Switching Level of Cascaded Multilevel Inverter

The H-bridges used to form cascaded multilevel inverter with three stages are considered. The DC sources V_{R1}, V_{Y1}, V_{B1} and V_{R2}, V_{Y2}, V_{B2} are connected with the H-bridge H_1 and H_2 respectively. The MS present in each phase is connected to DC source and the discontinued lines of second and third stage indicates that the replacement of DC source by ucap. Generally, 'n' number of cells can be connected in series and one source is enough per phase [18].

The proposed scheme is an efficient method for multilevel inverter producing high quality power. This is an excellent method where only one DC source has been used and is useful for vehicles such as electric scooter, electric cars, and home appliances etc. The voltage levels can be controlled easily by knowing the voltage of all the floating capacitors [19]. The voltage across the capacitor C_1 is $V_{m/2}$ and voltage across capacitor C_2 is $-V_{m/2}$. Each cells of the proposed inverter has 3–levels, eventhough the multiplying effect of 3 cells produces 27-levels if the voltage is set appropriately. The voltage source V_m which is three times greater than the source voltage of first auxiliary H-bridge (H_1) connected to all the three phases. The battery voltages V_{R1}, V_{Y1}, and V_{B1} are two times greater than the voltages V_{R2}, V_{Y2}, and V_{B2} (here the battery source is replaced by ultracapacitor so both the voltages are equal in this case). Further, the suffix indicates phase of the motor. For example, if $V_{C1}=V_{C2}=108V$, $V_{R1}=V_{Y1}=V_{B1}=36V$ and $V_{R2}=V_{Y2}=V_{B2}=18V$. This method automatically reduces the number of additional sources so that it will also reduce the weight and increase the life of the particular system (refer table 1).

Table 1. Comparison of battery versus ultra-capacitor [15]

Parameters	Battery	Ultracapacitors
Energy Density (Wh/Kg)	10-100	1-10
Specific Power (W/Kg)	< 1000	< 10000
Charge Time	1-5 hrs	0.3-30 S
Discharge Time	0.3-3 hrs	0.3-30 S
Life Time	1-5 Years	10-12 Years

The structure of cascaded multilevel inverter with single source is shown in Fig. 2.

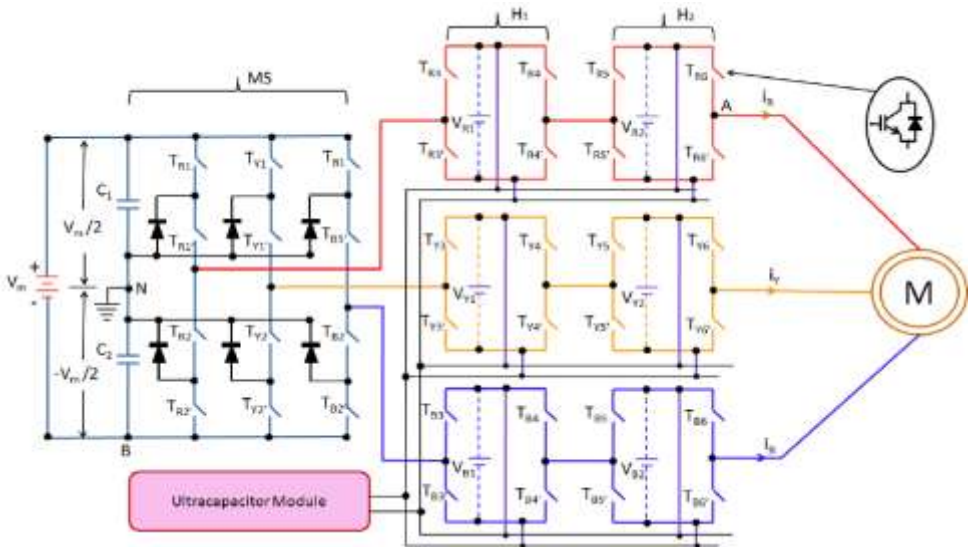

Figure 2. Cascaded 27 level inverter with ultracapacitor source

The capacitor connected in the inverter affects the 3-phases (R,Y,B) through the switching transistors T_{R1}, T_{R2} and T_{R3}. In the switching transistor the suffix R, Y, B denotes three different phases and 1, 2, 3 represents the count number respectively. The capacitor C_1 makes T_{R1} OFF and T_{R2} ON through the clamped diode and the complement transistors T_{R1}' and T_{R2}' performs the complement of the above [20]. In real time implementation, a fixed delay is provided between the transistor T_{R1}, T_{R2} and its complements T_{R1}' and T_{R2}'. In this study we consider small delay (25 micro second) between both the transistor pairs. If the voltage is negative with respect to mid-point (N), the current i_R flows through the junction A by the capacitor C_1, if it is positive the current i_R flows through C_2.

3.2.Switching Level of Cascaded Multilevel Inverter

The voltage level between A and N is $V_{AN} = V_m/2$, $V_{BN}=-V_m/2$. For voltage level $V_m/2$, the switches T_{R1}, T_{Y1}, and T_{B1} are turned ON; for the voltage level $-V_m/2$, the complementary to the above set will turned ON. A small delay of 25 micro second was given between each switch and its complements. The switching level of MS, H_1, and H_2 of R-Phase output with respect to N is written in the following condition:

$$V_{AN} = \begin{cases} -\frac{V_m}{2}, & T_{R1} = 0 \\ 0, & T_{R1} = 1 \\ \frac{V_m}{2}, & T_{R1} = 2 \end{cases} \quad (1)$$

This topology has 27-voltage levels and the switching states of MS, H_1, and H_2 are varying according to (1). The switch set of MS for R-phase varies 3 states, the switches of H_1 of R-phase varies 3 distinct state for each state variation of MS and the switches of H_2 of R-phase varies 9 distinct states of each state variation of MS [21] and [22]. According to (1), the different switching conditions and the voltage between R-phase to mid-point are as follows:

state (i) : MS=0, H_1 and H_2 has different states as:

$H_1 = H_2 = 0$; $V_{AN} = -V_m/2 - V_{R1} - V_{R2}$

$H_1 = 0, H_2 = 1$; $V_{AN} = -V_m/2 - V_{R1}$

$H_1 = 0, H_2 = 2$; $V_{AN} = -V_m/2 - V_{R1} + V_{R2}$

$H_1 = 1, H_2 = 0$; $V_{AN} = -V_m/2 - V_{R2}$

$H_1 = 1, H_2 = 1$; $V_{AN} = -V_m/2$

$H_1 = 1, H_2 = 2$; $V_{AN} = -V_m/2 + V_{R2}$

$H_1 = 2, H_2 = 0$; $V_{AN} = -V_m/2 + V_{R1} - V_{R2}$

$H_1 = 2, H_2 = 1$; $V_{AN} = -V_m/2 + V_{R2}$

$H_1 = 2, H_2 = 2$; $V_{AN} = -V_m/2 + V_{R1} + V_{R2}$

state (ii) : MS=1, H_1 and H_2 has different states as:

$H_1 = H_2 = 0$; $V_{AN} = -V_m/2 - V_{R2}$

$H_1 = 0, H_2 = 1$; $V_{AN} = - V_{R1}$

$H_1 = 0, H_2 = 2$; $V_{AN} = - V_{R1} + V_{R2}$

$H_1 = 1, H_2 = 0$; $V_{AN} = - V_{R2}$

$H_1 = 1, H_2 = 1$; $V_{AN} = 0$

$H_1 = 1, H_2 = 2$; $V_{AN} = V_{R2}$

$H_1 = 2, H_2 = 0$; $V_{AN} = V_{R1} - V_{R2}$

$H_1 = 2, H_2 = 1$; $V_{AN} = V_{R1}$

$H_1 = 2, H_2 = 2$; $V_{AN} = V_{R1} + V_{R2}$

state (iii) : MS=2, H_1 and H_2 has different states as:

$H_1 = H_2 = 0$; $V_{AN} = V_m/2 - V_{R1} - V_{R2}$

$H_1 = 0, H_2 = 1$; $V_{AN} = V_m/2 - V_{R1}$

$H_1 = 0, H_2 = 2$; $V_{AN} = V_m/2 - V_{R1} + V_{R2}$

$H_1 = 1, H_2 = 0;\ V_{AN} = V_m/2 - V_{R2}$

$H_1 = 1, H_2 = 1;\ V_{AN} = V_m/2$

$H_1 = 1, H_2 = 2;\ V_{AN} = V_m/2 - V_{R2}$

$H_1 = 2, H_2 = 0;\ V_{AN} = V_m/2 + V_{R1} - V_{R2}$

$H_1 = 2, H_2 = 1;\ V_{AN} = V_m/2 + V_{R2}$

$H_1 = 2, H_2 = 2;\ V_{AN} = V_m/2 + V_{R1} + V_{R2}$

3.3. Ultracapacitor

Power electronics are playing a key role in power conversion systems such as renewable sources, industrial drives, home appliances, transportation, power generation etc. These applications require a device which has short time for storage and restoration of energy. The total charging and discharging time should be around tens of seconds. The ucap is fit for this purpose. Ucaps have high energy which is several times greater than that of traditional capacitors. It does not have any chemical reaction, and the number of charging and discharging cycles are 3500 times greater than that of battery. For the proposed multilevel inverter topology, we can replace the DC sources by ucaps. Batteries are used in high power applications but are replaced frequently; the ucaps provides solution through better life time and reliability. The equivalent circuit model of ucap [4] and [23] is shown in Fig. 3.

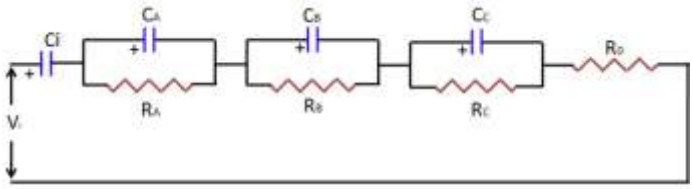

Figure 3. Equivalent circuit model of ultacapacitor

For a UC, three types of models are familiarly used: the dynamic model, the classic model, and the multi-stage ladder model. Here we used dynamic model based on [28]. The model consists of a series resistance, three RC networks and a bulk capacitance. The transient behavior of Ucap can be captured by the dynamic model over a wide range of frequencies. The output equation with continuous time state space equation are given by

$$\begin{bmatrix} \frac{du_1}{dt} \\ \frac{du_2}{dt} \\ \frac{du_3}{dt} \\ \frac{du_4}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R_A C_A} & 0 & 0 \\ 0 & 0 & -\frac{1}{R_B C_B} & 0 \\ 0 & 0 & 0 & -\frac{1}{R_C C_C} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \end{bmatrix} + \begin{bmatrix} \frac{1}{C_i} \\ \frac{1}{C_A} \\ \frac{1}{C_B} \\ \frac{1}{C_C} \end{bmatrix} \mathrm{i} \qquad (2)$$

Where $V = u_o + u_1 + u_2 + u_3 + R_s i$, u_0 denotes the bulk capacitance, u_1,u_2 and u_3 represent the voltages of the three RC networks, Rs represents the series resistance and V is the output voltage. According to (2), the values of resistance and capacitance were computed and are shown in Table 2.

Table 2. Estimated resistance and capacitance values

Capacitance (F)		Resistance (Ohm)	
Ci	2528	R_A	5.28×10^{-4}
C_1	752	R_B	7.91×10^{-5}
C_2	978	R_C	7.24×10^{-5}
C_3	1245	R_0	6.37×10^{-4}

3.4. State of charge

The state of charge (SOC) of the ucap can be modeled by using Ceraolo model and each elements of the circuit should be identified by various SOC [24]. Here we are considering a lead-acid battery which can draw the charge with constant discharging current. The measurement of capacity also depends on the discharging voltage. The capacity of the battery at constant discharge current (I) and constant electrolytic temperature β (^{o}C) can be expressed as:

$$C(I,\beta) = \mathrm{C_o(I)}\left(1+\frac{\beta}{\beta_f}\right) \qquad (3)$$

Where β_f is the freezing temperature of electrolyte normally the value is assumed at -40^{o}C, C_o is an empirical function of discharge current. Moreover, according to [24] C_o(I) can be expressed with respect to the reference current I* as:

$$C_o(I) = \frac{\mathrm{K_c}C_o^*}{1+(K_c-1)\left(\frac{I}{I^*}\right)^{\gamma}} \qquad (4)$$

Where K_c and γ are empirical coefficients, the value is constant for a given battery and the corresponding value of I^*. Equation (4) provides good results in a wide range of currents around I^*. The equations (3) and (4) are applicable when the current and electrolyte temperature are constant. During transients the filtered current I_{avg} must be taken and the capacity for the actual electrolyte temperature, $C=C(I_{avg},\theta)$. The SOC of the battery can be calculated from the charge and capacity with a given temperature as:

$$SOC = 1 - Q_B / K_c C(\mathrm{I}^*) \qquad (5)$$

The depth of discharge (DOD) of battery is given by

$$DOD = 1 - Q_B C(I_{\mathrm{mean}},\theta) \qquad (6)$$

where Q_B is the available charge of battery, $Q_B(t) = \int_0^t -I_m(t)dt$, C is the capacity of battery, and I_{mean} is the mean discharge current.

3.5. Battery Sizing

The batteries present in the H-bridge cells are replaced by ucap module (refer Fig. 2). If the capacitors are not present, the battery size must meet the peak current in the discharging period. Most of the multilevel techniques used only DC source as supply voltage. In that case, the battery pack can be calculated as

Battery pack size = (Ah requirement x duration)/DOD

In this study we used ucaps as DC source so the battery pack size becomes

battery pack size = Average current x Discharge period

3.6. Ucap Sizing

The life time of ucap is much greater than that of battery and it delivers the maximum current for the duration 12-15 minutes which depends on the manufacturer. The sizing of ucap is slightly different from the battery and the voltage drop must be taken into account here. A 1000 F Maxwell ucap with series resistance of 0.04 Ohm has been taken for sizing. It must be properly selected for design in such a way that the voltage drop should be within the load limit. In series and parallel connections, discharging period and the resistance also affect the voltage drop of the ucap and it is given as:

$$V_d = \frac{\mathrm{IC}_S}{C_P}\left(\frac{D_P}{C}+R\right) \qquad (7)$$

where V_d is the voltage drop, C_s is number of capacitors in series, C_p is number of capacitors in parallel, R is the equvalent resistance in series, and D_p is the discharging period.

3.7. Capacitor Voltage Control

The voltage level of ucaps present in H_1 and H_2 should be maintained and it is a difficult task. The cascaded multilevel inverter control is based on the PWM that adjust the ON and OFF time of the inverter. The adaptive control mechanism used to control the capacitor voltage is shown in Fig. 4.

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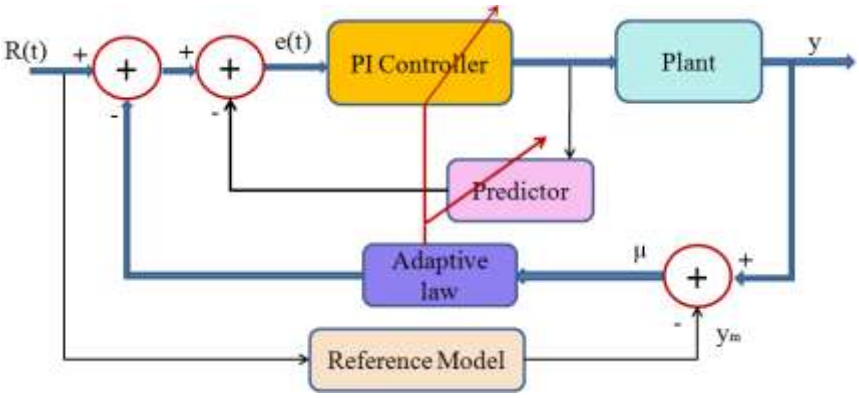

Figure 4. Adaptive ultracapacitor voltage control

The error between the reference and measured voltage of ucap of H-bridge is processed by the PI tuning mechanism. It is a robust tuning system for the PI controller. The PI tuning strategy can be adjusted by the parameters of PI controller as a result charge and discharge of ucap. The capacitor voltage of all the three phases can be done by using this closed loop regulation.

We consider the ultracapacitor dynamics and uncertainties, and a predictor is introduced to model time delay, in addition to PI controller [32,33]. If the time constant, T_c is assumed to be known and the plant dynamics is expressed as:

$$P(S)=\frac{\gamma}{S+\gamma}\ e^{-T_d S} \qquad (8)$$

In this work, the time delay of the plant is known and T_c can be derived from (1) in terms of the plant parameter γ, therefore, $T_c=\frac{1}{\gamma}$.

The predictor transfer function is given by

$$SP(S)=\frac{\gamma}{S+\gamma}\left(1-e^{-T_d S}\right) \qquad (9)$$

Hence (8) and (9) can be written as

$$\hat{S}P(S)=\frac{1}{\hat{T}_c S+1}\left(1-e^{-T_d S}\right) \qquad (10)$$

Now we represent the estimate of γ and T_c by $\hat{\gamma}$ and $\hat{T}_c$, the predictor can be constructed by

$\hat{C}(s)$, the close loop transfer function of the system from the reference signal, γ to the system response. The adaptive PI controller can also be represented by the relation $\hat{k}_p=\frac{k_i}{\hat{\gamma}}$ as

$$\hat{C}(S)=\frac{k_i}{\hat{\gamma}s}\frac{s+\hat{\gamma}}{s}=k_i\frac{\hat{T}_c s+1}{s} \qquad (11)$$

We assume that the plant parameters slowly change with respect to time and the output, y can be represented as a function of reference signal as:

$$y=\frac{P(s)\hat{C}(s)}{1+\hat{C}(s)\hat{S}P(s)+P(s)\hat{C}(s)}\alpha \qquad (12)$$

By using instantaneous cost function [33], $J(\hat{T}_c)=\frac{\mu^2}{2}$, and the adaptive law based on gradient algorithm is expressed as

$$\hat{T}_c=-\alpha\nabla J(\hat{T}_c)=-\alpha\mu\frac{\partial\mu(\hat{T}_c)}{\partial(\hat{T}_c)} \qquad (13)$$

Where the estimation error, μ=y-y_m, the adaption gain, α > 0. We now that y_m is independent of $\hat{T}_c$, therefore, $\frac{\partial \mu}{J\hat{T}_c} = \frac{\partial y}{\partial \hat{T}_c}$ and (13) can be expressed as

$$\hat{T}_c = -\alpha\mu \frac{\partial y}{\partial(\hat{T}_c)} \tag{14}$$

The value of μ can be measured once we know the value of y and y_m. The adaptive law can be implemented by knowing $\frac{\partial y}{\partial(\hat{T}_c)}$. Now the output y can be written in terms of $\hat{T}_c$ as:

$$y = \frac{\frac{k_i}{s}\frac{\hat{T}_c\,s+1}{T_c\,s+1}e^{-T_d s}}{1+\frac{k_i}{s}\left[1-\left(1-\frac{\hat{T}_c\,s+1}{T_c\,s+1}\right)e^{-T_d s}\right]}\alpha \tag{15}$$

For simplification, $v = \frac{\hat{T}_c\,s+1}{T_c\,s+1}$, and the partial derivative, $\frac{\partial m}{\partial(\hat{T}_c)} = \frac{s}{T_c\,s+1}$, now (15) becomes

$$y = \frac{k_i v e^{-Tds}}{s + k_i\left[1-(1-v)e^{-Tds}\right]}\alpha \tag{16}$$

Now the partial derivative of y with respect to m is given by

$$\frac{\partial y}{\partial v} = \frac{k_i e^{-Tds}\left[s + k_i(1-e^{-Tds})\right]}{(s + k_i\left[1-(1-v)e^{-Tds}\right])^2}\alpha \tag{17}$$

$$\frac{\partial y}{\partial \hat{T}_c} = \frac{s + k_i(1-e^{-Tds})}{s + k_i\left[1-(1-v)e^{-Tds}\right]\hat{T}_c s+1}\alpha \tag{18}$$

The sensitivity of gradient based adaptive law cannot be computed because the value of v contains an unknown, $\hat{T}_c$. Now we define $v \cong 1$, and (18) becomes

$$\frac{\partial y}{\partial \hat{T}_c} \cong \frac{s + k_i(1-e^{-Tds})}{s + k_i}\frac{s}{\hat{T}_c s+1}y \tag{19}$$

Now the adaptive law based on (13) becomes

$$\hat{T}_c \cong -\alpha\mu\left(1-\frac{k_i e^{-Tds}}{s + k_i}\right)\frac{s}{\hat{T}_c s+1}y \tag{20}$$

IV. SIMULATION AND EXPERIMENTAL RESULTS

4.1. Simulation Results

The simulation was developed by using Simulink tool which is present in Matlab 2015. The components such as battery, ucaps, and delays etc. have been developed and interface with the power electronics. The output was taken from A-N for R-phase ie: phase to mid point. Before integrating all the components, we have to identify proper functionality of each component. The performance of battery model is compared with the dynamic model of battery explained by Ceraolo [24]. The battery parameters used for the simulation model is given in Table 3.

Table 3. Different parameters of battery and ucap used for simulation

Parameters	Without Ultracapacitor	With Ultracapacitor
Battery Capacity (Ah)	190	92
Battery Pack Voltage (V)	12.5	12.5
Discharging Time (hours)	10	10
Ultracapacitor cell Capacitance (F)	-	400
Ultracapacitor cell voltage (V)	-	2.7
Ultracapacitor bank capacitance (F)	-	15080
Capacitance Tolerance (%)	-	+/- 10
Number of cells in series	-	5
Equivalent Series Resistance (milliohms)		3.2

Comparison of harmonic analysis is made between the proposed with other methods such as hybrid cascaded multilevel inverter (HCMI) [29], phase shift and step wave modulation applied to symmetrical cascaded multilevel inverter (SCMI) [30] and an experimental investigation of multilevel inverter with digital controller (MIDC) [31]. The performance is also compared with these three methods with the proposed method through various parameters measured by simulation.

During discharge, the battery will supply enough voltage and it will acts as an open circuit voltage when the load is ideal. The measured and modeled voltage is as shown in Fig. 5.

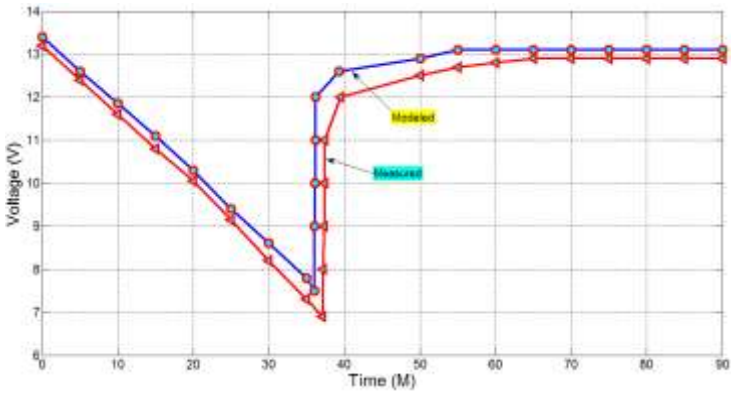

Figure 5. Comparison between modeled and measured voltage of battery

It illustrates that the model under both the load and no-load conditions and one can easily understand that the battery voltage takes around 3 seconds to reach its no-load. It was observed that the model produces less than 2% error for all the simulation times. A single cell voltage and current of battery and ucap module is shown in Fig. 6 and 7 respectively.

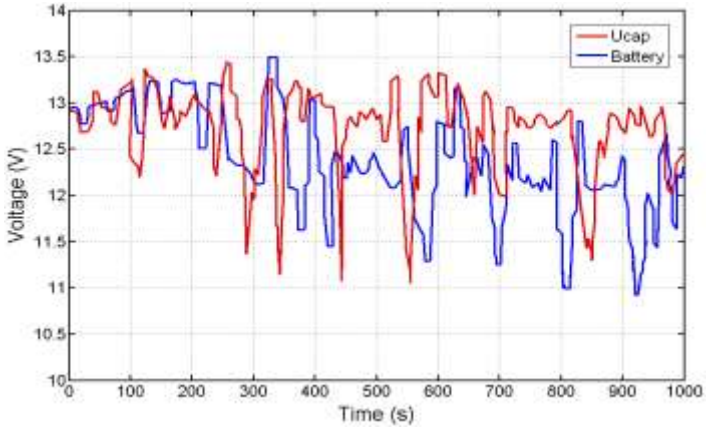

Figure 6. Measured voltage of battery and ucap module

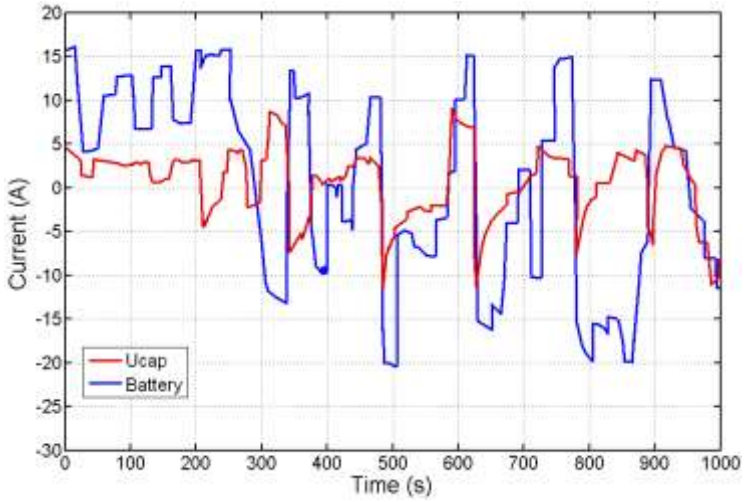

Figure 7. Measured current of battery and ucap module

The voltage of ucap varies more than that of battery voltage under load condition. The battery current is more fluctuating than that of ucap. During starting time of load, the current of both the battery and ucaps are almost constant and after that both are varying according to the load.

The simulation was performed for the multilevel inverter by using DC sources and the source of H-bridges is replaced by ucap. The simulink model for the 27- level cascaded multilevel inverter is shown in Fig. 8.

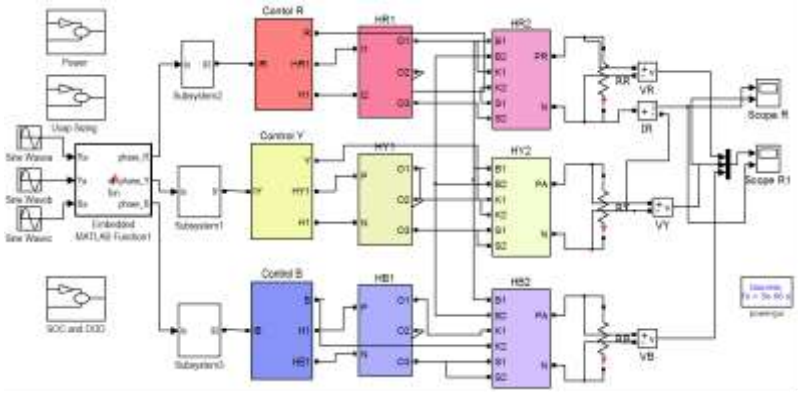

Figure 8. Simulink Model for Single DC source cascaded multilevel inverter

The sizing of battery was done and the maximum capacity is 100Ah for this case. The ucap is sized in such a way that the maximum current of 65A will be for 12 minutes. The ucap cells of 400 F combined with a bank of 6000 F was used in the simulation. In the multilevel inverter testing, the SOC of the battery is considered as it was fully charged initially. The current, voltage, harmonic distortion, and the SOC of both the ucap and the battery present in the multilevel inverter were studied. The output voltage of 3-phase cascaded multilevel inverter and current for the corresponding R-phase with all DC source is shown in Fig. 9.

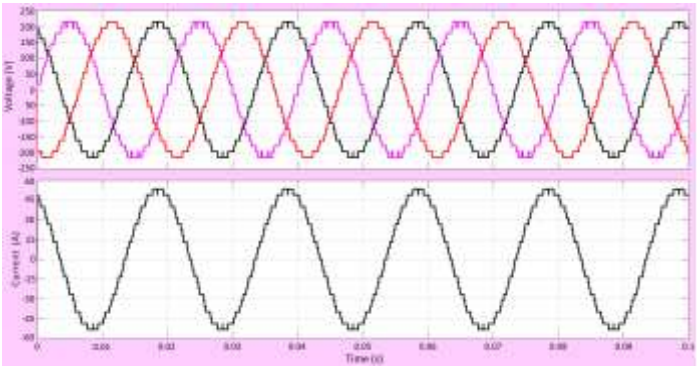

Figure 9. Output voltage of 3-phase inverter with R-phase current (all DC source)

The 3-phase output voltage and the corresponding R-Phase current is taken. Here the voltage sources were used with the ratio 1:1/3:1/6. The voltage source of MS =108V, H_{R1} = 36V, and H_{R2} = 18V. The output waveform has 27 levels and it

produces very less distortion. The output voltage and current waveforms of a 3-phase cascaded multilevel inverter with ucap as source is shown in Fig. 10.

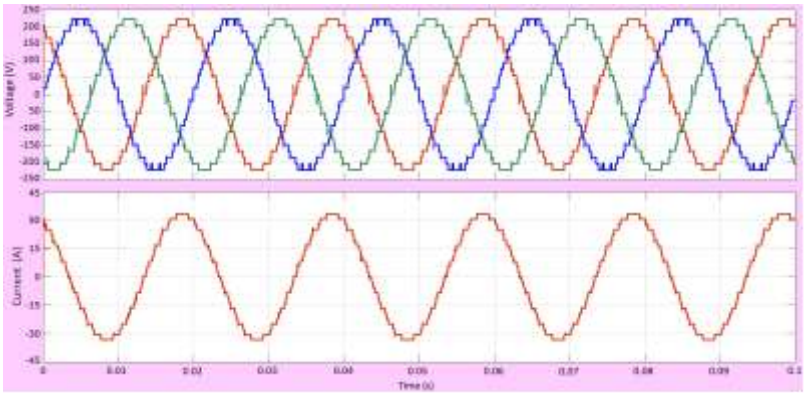

Figure 10. Output voltage of 3-phase inverter with R-phase current (single DC source)

The 3-phase output voltage and the corresponding R-Phase current is measured. Here the voltage sources were replaced by ucaps with the values $C_1 = C_2 = 2700$ F, $C_{R1} = 985$ F, and $C_{R2} = 1240$ F are taken from the bank.

The supply voltage is set in such a way that the voltage of $C_1 = C_2 = MS$, $C_{R1} = MS/3$, and $C_{R2} = MS/6$. Here we choose the voltage of $C_1 = C_2 = 108$V, $C_{R1} = 36$V, and $C_{R2} = 18$V. In this method, the single DC source cascaded multilevel inverter generates 27 levels in the output. Here the 6 DC sources which were present in H_1 and H_2 have been replaced by ucaps and this will reduce the energy utilization up to 36% of the total power. Moreover the ucaps will not suffer deep discharge in their life time as like a battery. The capacitors produces ripple in the output waveform and it is around 8.96%

The output voltage and their corresponding Fourier harmonic spectrum of R-phase (A-N) for HCMI, SCMI MIDC and the proposed method are shown in Fig. 11.

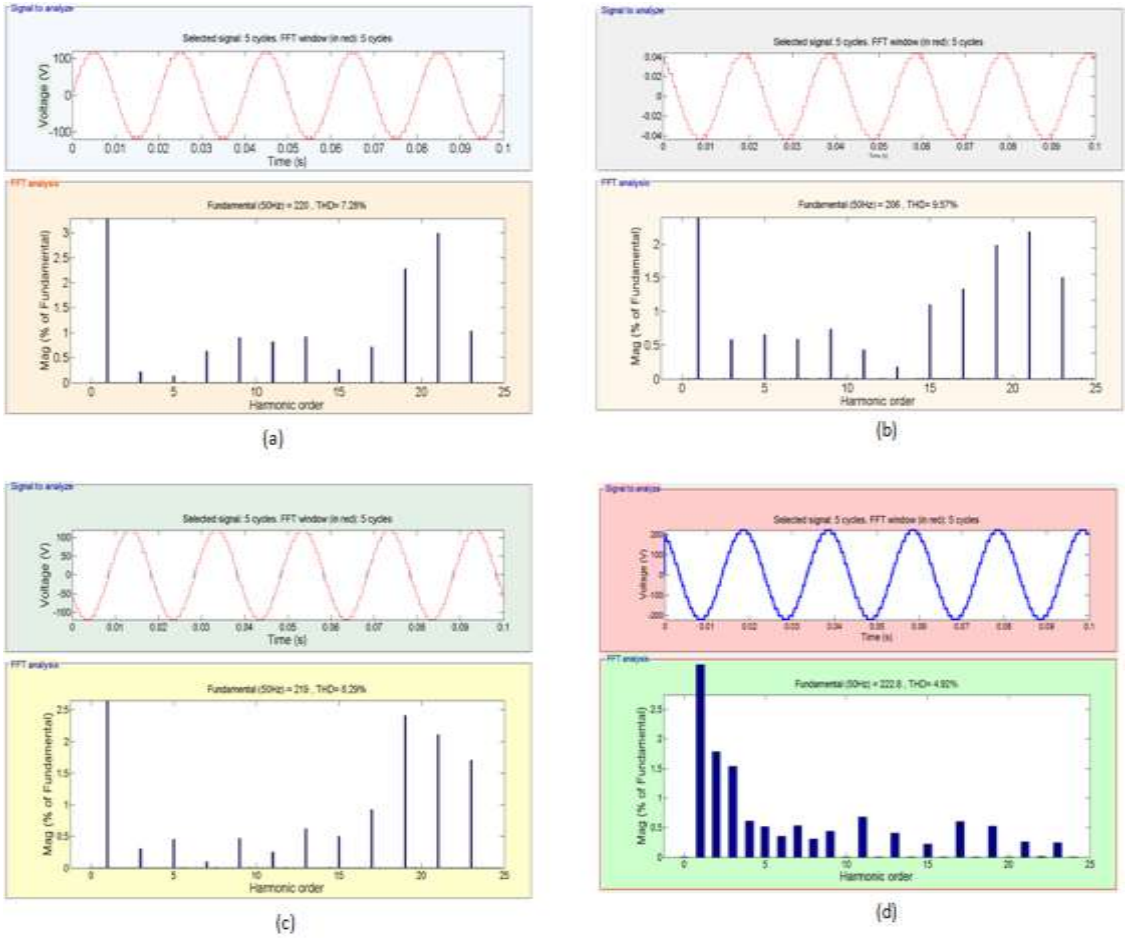

Figure 11. Output voltage of R-phase and corresponding harmonic spectrum (a) HCMI (b) SCMI (c) MIDC and (d) proposed method

The THD of the output voltage is 7.28%, 9.57%, 8.29% and 4.65% for HCMI, SCMI, MIDC and the proposed method respectively. The multilevel inverter output is connected with a non linear RLC load has the values (R=10 kΩ, L=.01mH, C=10μH). The non-linear load produces harmonics in the output of the multilevel inverter. On comparing fig. 11 (a)-(c) and the proposed method, has the THD is 4.65 and it is very less compared to other methods. The output current and their corresponding Fourier harmonic spectrum of R-phase for HCMI, SCMI, MIDC and the proposed method are shown in Fig. 12.

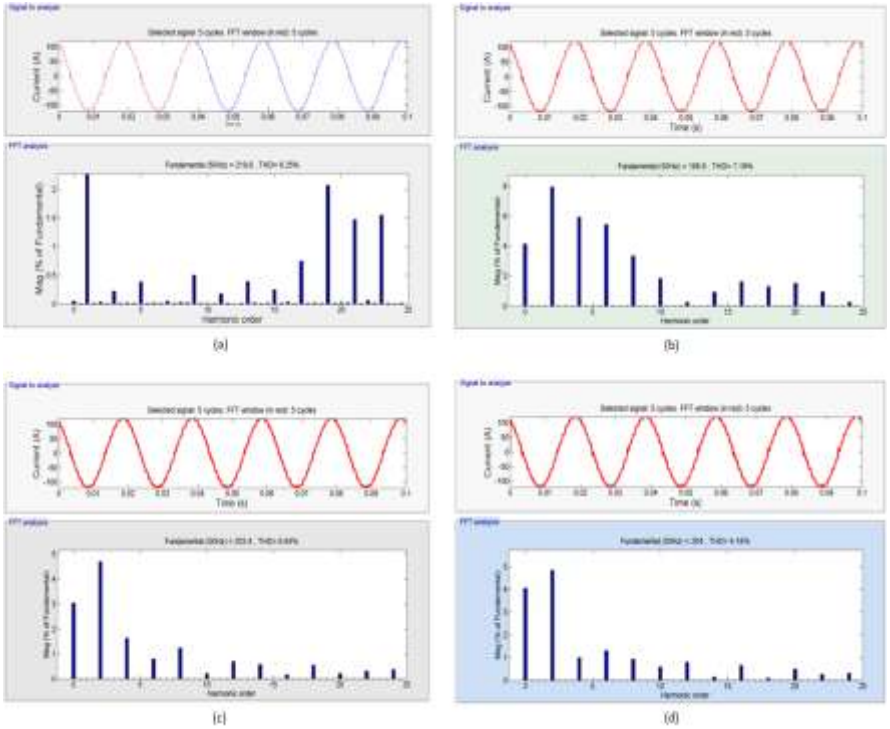

Figure 12. Output current of R-phase and corresponding harmonic spectrum (a) HCMI (b) SCMI (c) MIDC and (d) proposed method

The THD of the output current 6.25%, 7.19%, 6.84% and 4.16% for HCMI, SCMI, MIDC and the proposed method respectively. On comparing fig 12 (a)-(c) and 12 (d), the proposed method has THD of 4.16% and it is very less compared to other methods.

The current utilization is less compared to the previous method. The output voltage of the inverter is passed though a filter and the active and reactive power was measured and is shown in Fig. 13.

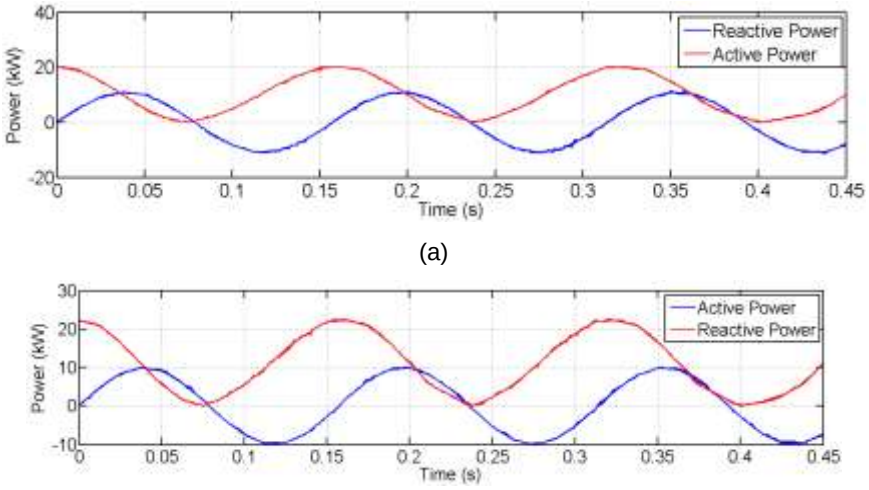

Figure 13. Active and reactive power (a) DC source (b) with ucap

It is noted that the active and reactive power for both the cases are almost equal. The ucap voltage variation under load condition is shown in Fig. 14.

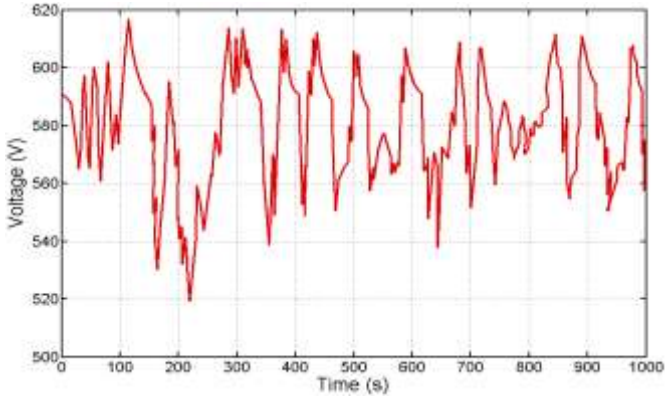

Figure 14. Terminal voltage of ucap bank under load

The terminal voltage of ucap is set around 620V and the simulation time step size is set as 0.1 second for simulation. The ucap voltage increases up to 618V when load increases and it decreases to a minimum of 520V when load get decreases.

The SOC of both the battery and ucap during simulation is shown in Fig. 15.

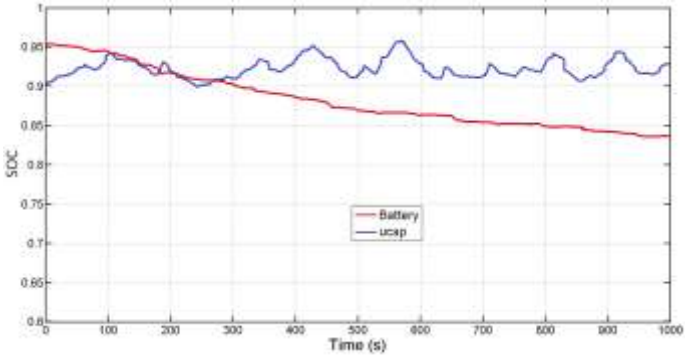

Figure 15. SOC of battery and ucap

Initially the SOC of both the battery and ucaps are full and it is around 90-95%. If battery voltage decreases then the DOD slowly increases. On the other hand the voltage of ucap will fluctuate under load but it will recharge and try to maintain the same level. It can be observed that the variation of SOC of ucap is less than that of battery. The SOC of ucap can be maintained between 84-90% because it automatically recharges the energy from the source. The SOC of battery is decreasing depending on the load. Comparison between both the multilevel inverters, using DC source such as HCMI, SCMI, MIDC and the proposed method using ucap with various load condition were obtained using Matlab FFT tool is presented in Table 4. We can observe that the quality of voltage and current depend on the total harmonic distortion (THD) [26] for both the cascaded multilevel inverter with DC source and by using ucap.

Table 4. Comparison of THD for different multilevel inverters under various load conditions.

Non linear load			THD (%)			
R (Ohms)	L (H)	C (F)	HCMI	SCMI	MIDC	Proposed
1	1exp(-5)	1exp(-8)	7.02	9.21	8.09	4.13
5	1exp(-4)	1exp(-6)	7.13	9.25	8.12	4.17
10	1exp(-2)	1exp(-4)	7.17	9.29	8.18	4.19
25	0.5	1exp(-2)	7.21	9.34	8.23	4.20
35	1.1	1exp(-1)	7.26	9.37	8.27	4.22
50	1.3	1.2	7.31	9.42	8.32	4.23
65	1.6	1.6	7.37	9.48	8.37	4.25
75	1.9	2.2	7.42	9.53	8.41	4.27

Table 4 shows that the harmonics of phase to mid-point voltage (V_{AN}) and current (I_{AN}) of R-phase. The overall power quality of both the inverter using DC source and ucap are slightly different from each other. The inverter using ucap as source produces less distortion than the inverter which uses DC source. On the other hand, the proposed method is very economical, less weight, and the total number of DC sources is reduced from 7 to 1. The system performance of multilevel

inverter which uses battery as source such as HCMI, SCMI, MIDC are compared with the proposed multilevel inverter is presented in Table 5.

Table 5. Performance comparison of different multilevel inverters with proposed method.

Parameters	HCMI	SCMI	MIDC	Proposed
Battery Size(Ah)	190	190	190	92
DOD (%)	42	38	40	18
Maximum battery Voltage (V)	13.5	13.5	13.5	13.25
Minimum battery Voltage (V)	10.8	10.8	10.8	12.1
Ultracapacitor cell voltage (V)	-	-	-	2.7
RMS Current (A)	15.5	14.2	14.9	10.2
Active Power (KW)	244.6	229.4	232.9	240.3
Reactive Power (KVAR)	32.7	37.3	35.8	38.4
Harmonic Power Loss (KW)	12.83	10.23	8.92	1.97
THD of Output Voltage in % of Fundamental Component	7.28	9.57	8.29	4.92
THD of Output Current in % of Fundamental Component	6.25	7.19	6.84	4.16

It is noted that the weight of the battery can be reduced with the usage of ucap and the life of ucap will be 3 times greater than that of DC source. Utilization of current can be reduced to 34% and the DOD can be reduced around 27% by the use of ucaps. When compare to the annual cost of the battery and ucap, 18% of cost will be saved by utilizing ucap [27].

Moreover, the output voltage of both seven DC source and single DC source methods are almost equal. But huge variation can be observed if this inverter is used in applications like electrical vehicles. The large variations can be tolerated by ucaps when acceleration or deceleration of EVs applied. The simulation results confirm that the proposed single DC source multilevel inverter is suitable for EV application.

4.2. Experimental Results

The experimental setup was constructed to verify the feasibility of the proposed method. Here scaled-down platform is used. To confirm the feasibility of the proposed multilevel inverter using ucap, the measured current and voltage waveform of both the methods such as multilevel inverter using battery as source and multilevel inverter using ucap as source is shown in fig. 16.

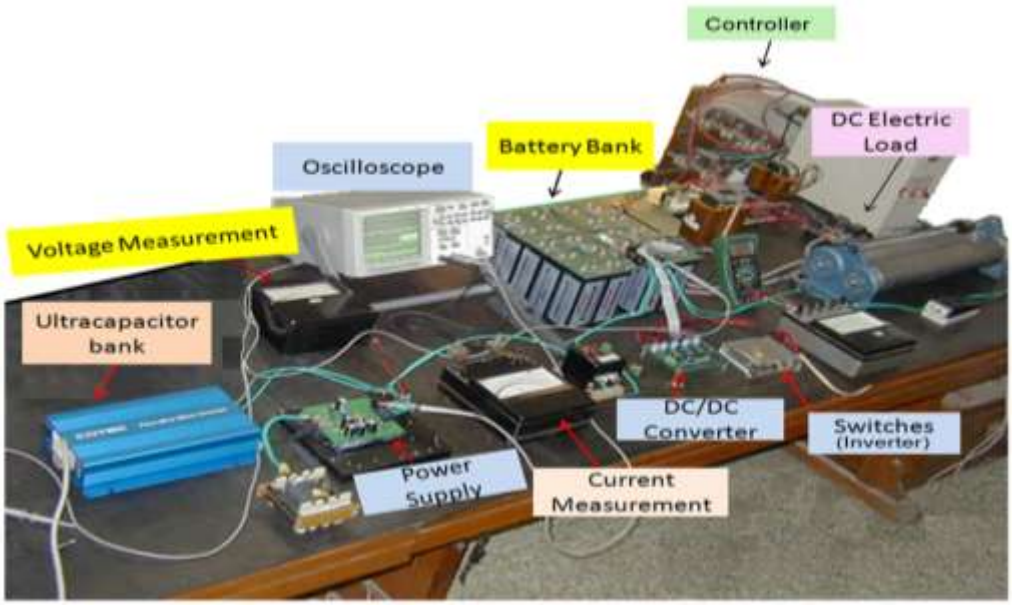

Figure : 16 Experimental Setup

The R-phase current and voltage waveform of both the multilevel inverters are shown in fig. 18(a) and (b) respectively.

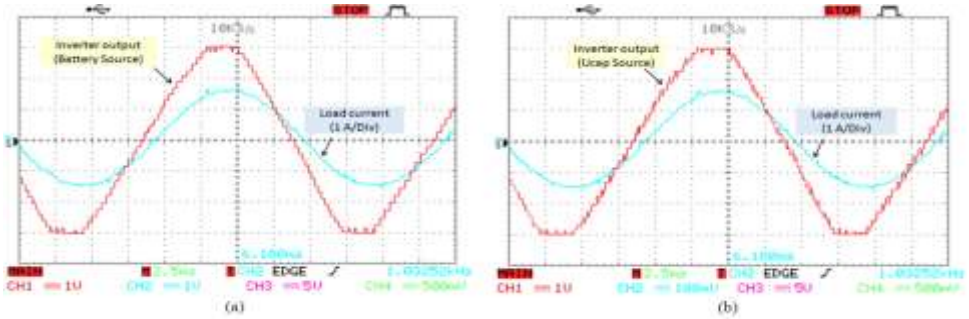

Figure 18. Experimental results of implemented 27-level inverter (a) Output voltage when battery as source (b) Output voltage when ucap as source.

It can be seen that, the voltage levels generated by the proposed multilevel inverter using ucap as source validates good performance and practicability.

Fig. 19 shows the experimental results of both the battery bank and ultracapacitor using PI controller.

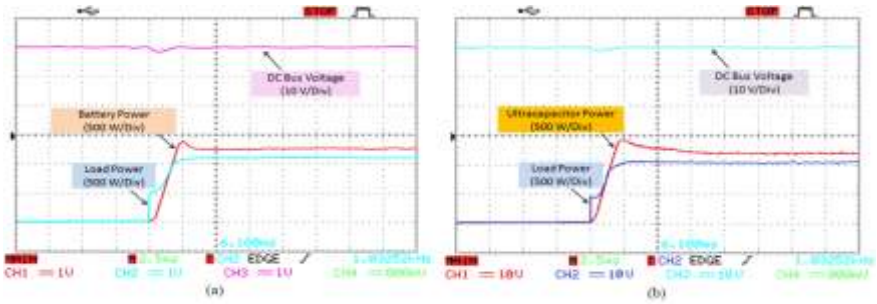

Figure 19. Experimental results: Performance of PI controller a) when battery as source (b) when ucap as source.

The performance of PI controller with battery source is shown in fig 19 (a). The predictor based controller has good convergence of DC bus voltage regulation to the reference voltage of 65V. The DC bus voltage sag is around 2% and it is very less compared to linear PI controller. The performance of PI controller with ucap as source is shown in fig 19(b). From the experimental output one can say that the performance of ucap is almost similar to battery sources.

A variable load is applied and the corresponding voltage and current waveform for both the battery and ucap as source are presented in fig. 20 (a) and (b) respectively.

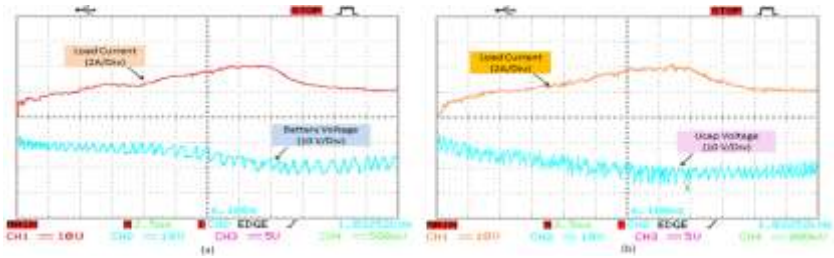

Figure 20. Performance of variable load (a) Current and voltage of battery as source (b) Current and voltage of ucap as source.

The voltage of both the battery and ucap decreases if load current increases. The performance of ucap source is almost equal to battery as source in multilevel inverter.

V. CONCLUSION

In this paper we proposed a multilevel inverter with all DC source and the voltage source of H-bridge is replaced by ucap. Various modulation techniques and numerous topologies found in the literature. An additional goal of this paper is to reduce the number of DC sources. Here we achieved a maximum of 27 levels by adjusting the capacitor voltage. The output and the harmonic order of both the multilevel inverter using all DC sources and H-bridge sources are replaced by ultracapacitor module is almost equal. The proposed ucap method produces ripple of 8.96% in the output. On the other hand, the energy utilization of ucap method can be reduced up to 36% and it will work 30% of float voltage. Then the

proposed method performances are compared to HCMI, SCMI and MIDC under various nonlinear load levels. In that the proposed method has 4.78% and HCMI, SCMI and MIDC are 5.5%, 7.25% and 6.86% respectively. The comparison results show that the proposed method which utilizes ucap is the most effective technique to reduce the harmonic present in the multilevel inverter. The proposed method reduces the number of sources as a result reduces the cost of the inverter and the total weight. These features make the system successful and can be utilized in EVs. The experimental results also confirm that the proposed ucap technique presented in this paper perform well and is suitable for electric vehicle. The output and the harmonic order are better than that of the previous methods. The proposed control scheme maintains the voltage level of capacitors and provides ripple free output without utilizing filters. This work can be extended to develop an efficient multilevel inverter for automobile applications using FPGA hardware.

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