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Power Efficient MAC Unit Based Digital PID Controllers

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ABSTRACT

Proper closed loop has been an ever hot issue in the automotive industry. The industrial equipments governed by PID controllers have very simple control architecture and efficiency but still they find a trouble dueto large power consumption and slow mathematical computation. Many researchers have worked out and are trying to design a low power, less delay PID. This paper reviews three MAC architectures with array, booth and wallace tree multipliers incorporated in PID architecture. The simulations are done and the area, power, delay results are synthesized using Xilinx ISE. Comparisons are made between these three architectures in terms of power delay product and area delay product.

Indexing terms/Keywords

Multiply-Accumulate (MAC), Array Multiplier, Booth Multiplier, Wallace Tree Multiplier, Proportional-Integral-Derivative controllers (PID).

INTRODUCTION

With the fast growth in the development of industrial equipments, engineers are in search of efficient control structures. Proportional-Integral-Derivative (PID) controller strongly captures its place in industries such as robotics, automation systems, aerospace and process control because of its very simple control structure, remarkable efficiency, robust performance and low power consumption. A PID will make the output plant to operate in the desired manner, causing the output to follow a reference input signal. For the proper tracking of output in relation to its reference, controllers are in need of less delay (i.e., quick computation of inner arithmetic operations) architectures. The various modules in controllers are designed with the help of state machines [1]. The looping of multipliers from controllers are shown in [2]. Seven adders based PID controllers and a vedic multiplier based controller are simulated and the results are compared for the efficient one [3]-[4]. The MAC flow diagram for various digital applications are shown [5]. This paper presents significant Multiplier-Accumulator (MAC) architectures with three different multipliers of PID which highlights on high speed, low power consumption. The comparisons are done among the multiplier, MAC unit and the PID architectures.

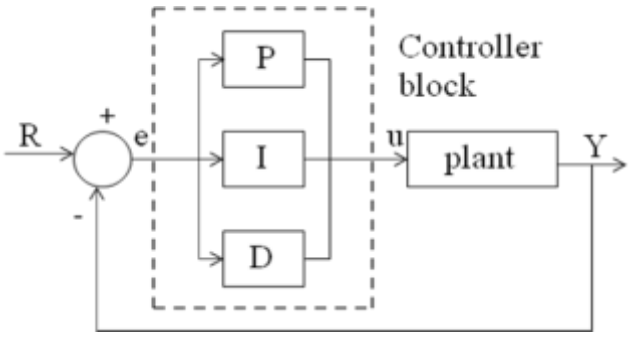

Fig.1. PID general architecture

The controller's output is the summation of proportional, integral and derivative gains which is given by,

$$u(t) = P(k) + I(k) + D(k) \quad (1)$$

The output equation is abbreviated with the error signal as

$$u(t) = K_p(e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{de(t)}{dt}) \quad (2)$$

Where, K_p is the proportional gain, T_i is the integral time constant and T_d is the derivative time constant. The block diagram of PID is depicted in Fig. 1.

Where, R, e and u represents the reference input, error signal and output of the controller. There are many tuning schemes are proposed for the efficient operation of PID controller. This paper gives special attention to the inner architecture especially on multiplier which decides the entire controller performance.

1.Multiply-Accumulator Block

The error signal which is calculated by subtracting the reference signal and the output is given as input to the multiplier. The adder receives input from the multiplier and the previously accumulated value from the shift register as shown in Fig.2. The choice of the multiplier depends on the application. Array multipliers usually have regular structures and are easy to expand. The partial products are generated by multiplying the multiplicand with their respective multiplier bits. The generated partial products are shifted according to their bit orders and then added as in Fig.3. Array multiplication needs to add as many partial products as there are in multiplier bits. The generation of A partial products requires A×B two-bit AND gates.

The multiplier utilizes more area for addition of N partial products which require (N-1)M bit adders. The array structure makes it difficult to measure the propagation delay.

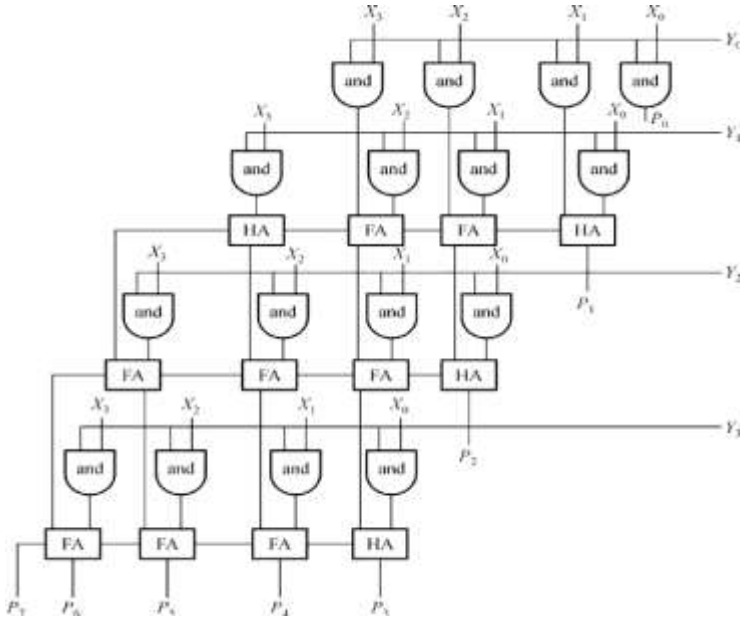

Fig.2. 4-bit array multiplier

A booth multiplier consists of a booth encoder, carry save adder tree to add partial products and a final adder for the result. This approach utilizes fewer additions and subtractions than that of straight forward algorithms. The partial products generated using booth encoder is given as input to the carry save adder so that sum and carry outputs are obtained. The number of partial products generated in booth algorithm is halved when compared to array multiplier. A wallace tree multiplier uses three steps for multiplying two numbers such as the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product. It is a tree multiplier with carry save adders as in Fig.3 which in turn consists of the most common ripple carry adders and full adders. The circuit layout is not easy but operating speed is high. The output from the multipliers is added with the previously accumulated value. The adder used here is the Ripple carry adder.

TABLE 1. BOOTH ENCODER

X_{i+1}	X	X_{i-1}	$Z_{i/2}$
0	0	0	+0*multiplicand
0	0	1	+1*multiplicand
0	1	0	+1*multiplicand
0	1	1	+2*multiplicand
1	0	0	-2*multiplicand

1	0	1	-1*multiplicand
1	1	0	-1*multiplicand
1	1	1	-0*multiplicand

A ripple carry adder is simply several full adders connected in series such that the carry can propagate through full adder before the addition. The carry propagation chain will determine the latency of the entire ripple carry adder circuit. A register is a group of binary storage cells (such as flip flops) capable of holding binary information. It also has the combinational part for data processing tasks. There are a group of flip-flops connected in a chain so that the output from one becomes the input of the next which. All the flip flops are driven by a common clock, and all are set or reset simultaneously. When there is a clock signal, the inputs D0,D1….D7 are loaded parallel into the register and the outputs Q0,Q1,….Q7 are also available in parallel at the output. All the data gets shifted simultaneously during a single clock cycle. Parallel shifting is much faster than serial shifting.

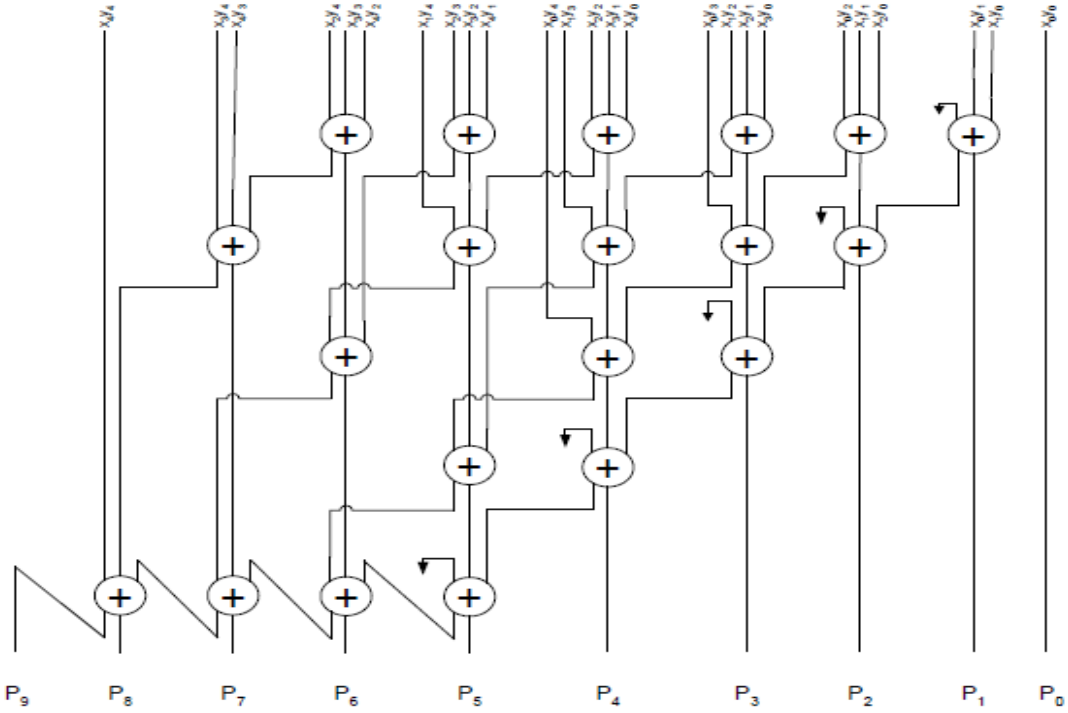

Fig.3. 4-bit Wallace Tree Multiplier

2.PID with Proposed MAC Unit

PID Controller is used in higher order dynamics. The two standard versions of PID are the incremental form and the commercial form. Both architectures are well suited for PID redundant architecture depending upon the application. In commercial form the transfer functions are approximated by limiting the derivative gain and setpoint weight. The designed MAC unit is embedded in the PID architecture. Due to quick computation of arithmetic operations, the controller is able to calculate its error value for next cycle. The designed PID can be used for various closed loop performance. $U_c(k)$ is the reference signal and Y(k) is the feedback stored in the register. The error signal is measured by calculating difference between the reference value and the previous value stored in the register. When there are four inputs, DMAC (Double MAC) instead of MAC is used to reduce the complexity.The coefficients of PID are utilized in the architecture as per the equations. The subtractor subtracts the two values and stored in a register for future operations as in Fig. 4. The commercial PID overcomes the drawbacks of incremental PID and can be used for all individual and combinations of controllers.

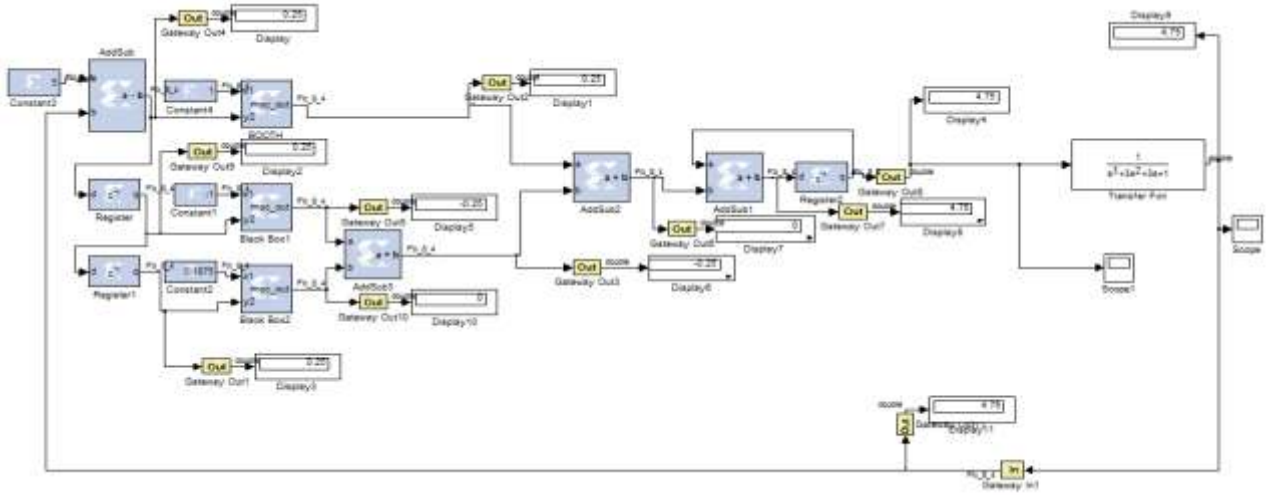

Fig.4. PID architecture based on Booth Multiplier

3. Results and Discussions

The VHDL coding for array, booth and wallace tree multiplier is written and their functions are verified using Modelsim 6.2c. The power results for these multipliers are synthesized using Xilinx ISE 13.2 and are tabulated.

TABLE 2.POWER RESULTS OF MULTIPLIERS

Multipliers	Power (mW)
Array	0.86
Booth	0.41
Wallace tree	0.64

The multiplier block output is given to a adder and an accumulator so that it constitutes a MAC unit for PID structure. The booth multiplier shows a better power result of 0.41mW when compared to array and wallace tree multipliers whics shows 0.86mW and 0.64mW respectively. Likewise the power analysis has been done for three MAC units and their comparisons done in the following tables.

TABLE 3. POWER COMPARISIONS OF MAC UNITS

MAC unit	Power (mw)
Array based MAC	58
Booth based MAC	50
Wallace-Tree based MAC	54

The power result shows that the MAC unit with booth multiplier has better performance than the other two multipliers. Using these MAC unit, the PID architecture are simulated in the System Generator.

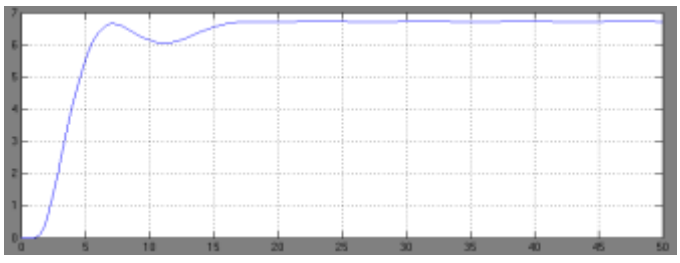

Fig 5. Waveform of array based incremental PID

In array based PID and wallace tree based PID, peak overshoot and steady state condition occur after a particular time asin Fig 5 and Fig 7. Eventhough it reaches the steady state, slight deviations continues. Booth based PID a minimum overshoot and reaches a contant state quickly as shown in Fig 6.

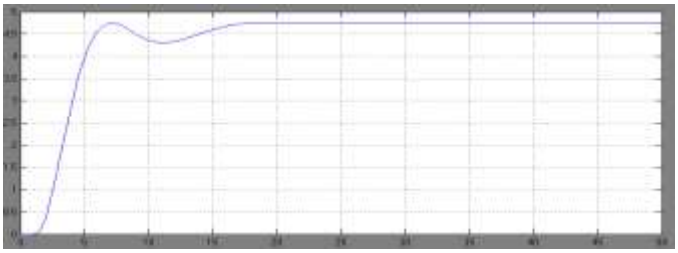

Fig 6. Waveform of booth based incremental PID

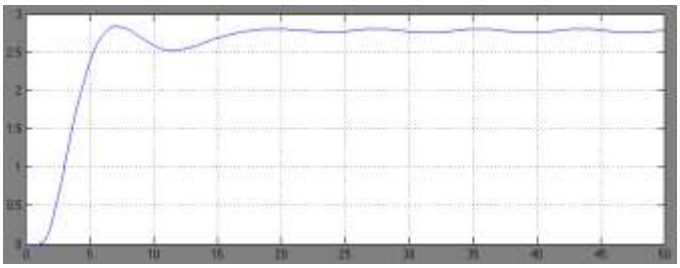

Fig 7. Waveform of Wallace tree based incremental PID

TABLE 4. PDP COMPARISION OF PID ARCHITECTURE

PID Architecture based on	Power (W)	Delay (ns)	Power Delay Product (PDP)
Array multiplier	0.464	3.556	1.649
Booth multiplier	0.39	3.506	1.367
Wallace tree multiplier	0.421	3.477	1.463

The booth multiplier based PID consumes less power and shows good power delay product. Wallace tree based PID depicts better result in terms of area. The booth based commercial PID also simulated as it consumes low power.

TABLE 5. AREA COMPARISION OF PID ARCHITECTURE

PID Architecture	Area (LUTs)
Array based PID	328
Booth based PID	380
Wallace tree based PID	320

The commercial architecture consumes same power as incremental but delay is slightly higher of 10ns because the structure is quite complicating.

5. Conclusion

Different multiplier based MAC unit has been designed and the power results are compared for better performance of PID controller. The booth based PID architecture consumes less power when compared to array based PID and wallace tree based PID architectures. The wallace tree PID architecture utilizes less area and delay than the other two. The power delay product(PDP) is better for booth architecture. So that the booth architectures will find its application in power constrain industries and wallace tree architectures will suit for area constrain industries.

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Author' biography with Photo

Dr.V.Kavitha started her career in teaching as a Lecturer in M. Kumarasamy College of Engineering with 3 years of service in Arts & Science College. She is currently Professor in Electronics and Communication Engineering of the same institution with more than 16 years. She graduated from Government College of Engineering, Salem in the stream of ECE followed by Masters in Computer and Communication Engineering from Periyar Maniammai College of Technology for Women, Tanjore. She did her Doctorate of Philosophy in Information and Communication Engineering from Anna University, Chennai.

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