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A Novel Design of Low-Power 1-Bit CMOS Full-Adder Cell Using XNOR and MUX

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ABSTRACT

This paper process a novel design for low power 1-bit CMOS full adder using XNOR and MUX, with reduced number of transistors using GDI cell. The circuits were simulated with supply voltage scaling from 1.2V to 0.6V &0.6V to 0.3V. To achieve the desired performance of power delay product, area, capacitance the transistors with low threshold voltage were used at critical paths and high threshold voltage at non critical paths. The results show the efficiency of the proposed technique in terms of power consumption, delay and area.

KEYWORDS

Power Delay Product, High and Low threshold voltages, parasitic capacitances, Area.

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1. INTRODUCTION

Full Adder circuits are popular in Very Large Scale Integration (VLSI) systems and have been employed in various Arithmetic and Logic Applications Viz. addition, subtraction and multiplication. Adders have become integral functional block in Digital signal processing, Image processing and Microprocessors applications and they also form the important circuitry of a CPU, floating point unit, cache and memory access unit. The design and the performance of the full Adder circuits are based on number of transistors, chip area, power dissipation, which has raised the need for low power and high speed, high performance and minimal area circuits [1-3]. The 1-bit full adder circuits proposed by Dan wag et.at[4], Y.Jiang et.at[5], Mahamoud et.at [6], and Lu Jamming et.at [7], it was observed, the circuit occupies low area, consumes low power and operates at lower operating voltage. It is difficult and even obsolete to keep full voltage swing operations the designs consider few transistors for low power consumption. This paper proposes a new implementation of 1-bit full adder with Gate-diffusion-input (GDI) based on MTCMOS and SCCMOS technique by reduction of parasitic capacitance through layout optimization [11-13].

2. PREVIOUS WORK

The GDI technique is a novel design which is very flexible for digital circuits; it helps in reduction of power and transistor count. The GDI cell has four terminals G, P, N and D, and uses two transistors for implementation of complex logic functions. The basic structure of GDI cell is shown in Fig. 1 and Table 1 describes the logical functions of GDI cell.

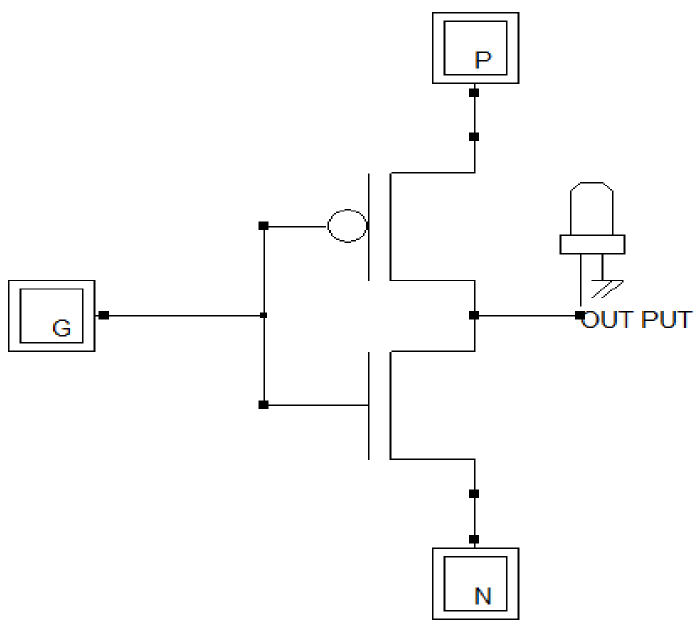

Fig. 1 Basic structure of GDI

Table 1 Logic functions implemented with GDI cell

N	P	G	D=output	FUNCTION
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

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GDI Based Full adder is shown in Fig. 2 and it shows the difference of implementation of logic functions from that shown in [10].

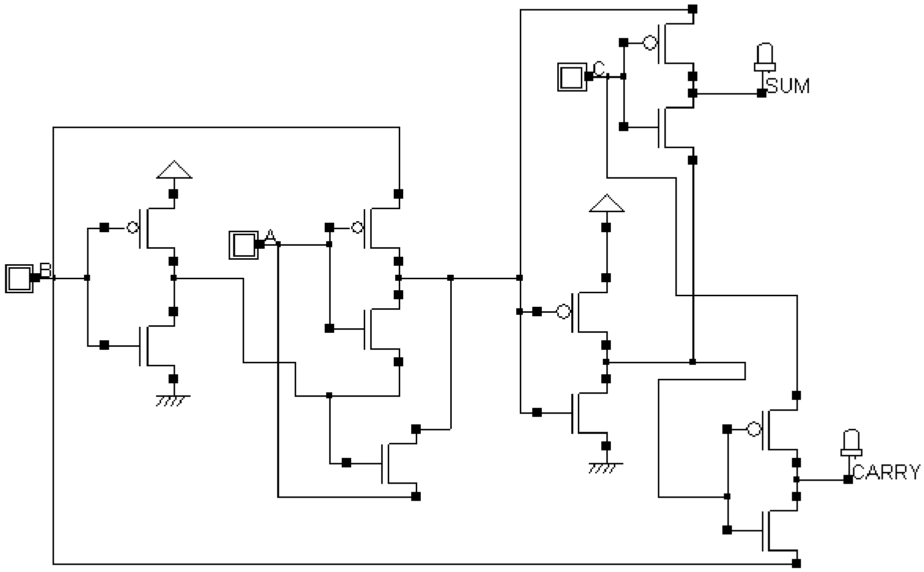

Fig. 2 GDI Based Full adder

3. PROPOSED WORKES

a) Proposed full adder:-1

A full adder was designed based on reduction of parasitic capacitance, with 10 MOS Transistor for the implementation of logic expression of Eq. (1), Eq. (2). The 1-bit full adder circuit consists of three modules, XNOR-I, XNOR-II and MUX. The XNOR-I and XNOR-II modules are designed using 4 MOS transistors considering two inputs and one output, and MUX module is designed with two MOS transistors for optimum operation. In comparison with design in [10], this technique uses fewer transistors, and in layout design parasitic capacitances are reduced to an optimum value without effecting the operation. Fig. 3 and Fig. 4 show the full adder implementation with 10 MOS transistors. The layout optimization and the simulated waveforms are indicated in Fig. 8 and Fig. 9 respectively.

$$Sum = \left(A \overline{\oplus} B\right) C_{in} + \left(A \oplus B\right) \overline{C}_{in} \quad (1)$$

$$C_{out} = \left(A \oplus B\right) C_{in} + \left(A \overline{\oplus} B\right) A \quad (2)$$

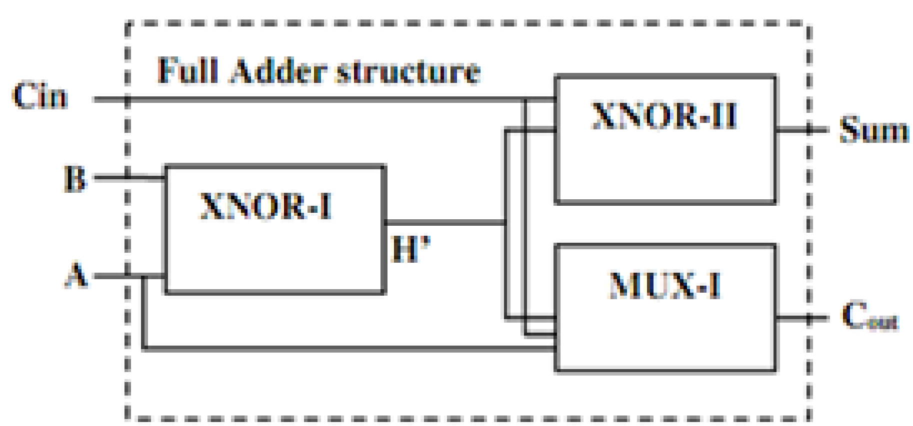

Fig. 3 Structure of Full adder

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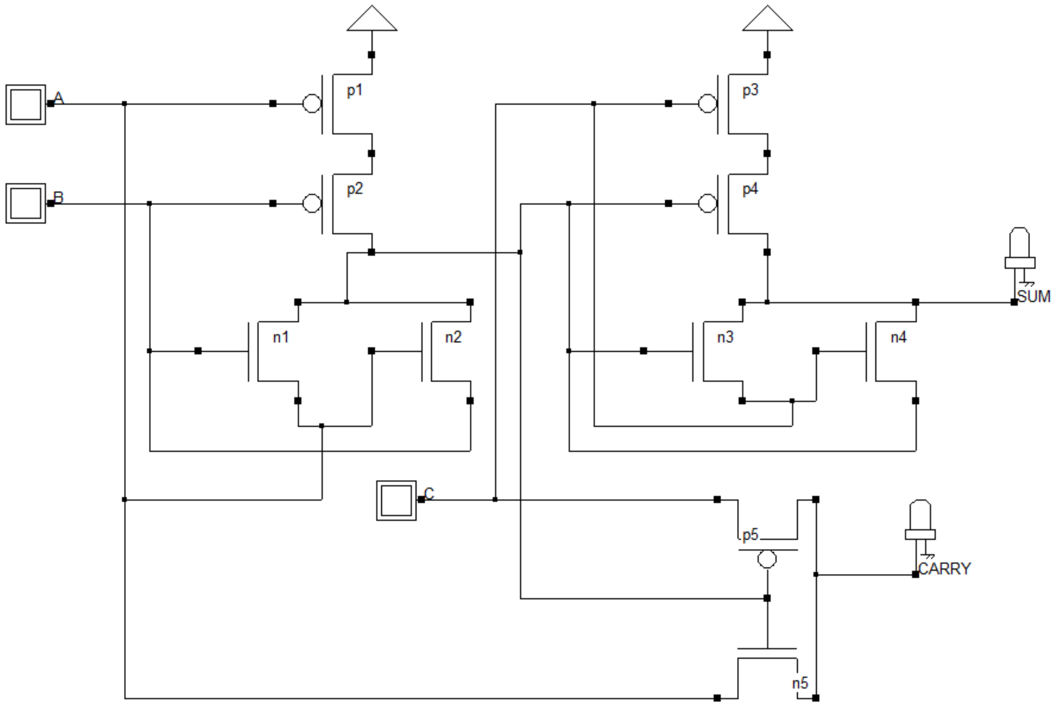

Fig. 4 Full adder implementation with10 MOS transistors

b) Proposed full adder:-2

An 8 transistor full adders was designed based on reduction of parasitic capacitance, power and area through layout optimization. The full adder consists three modules, XNOR-I, XNOR-II and MUX. The XNOR logic is implemented with 3 MOS transistors and MUX logic with 2 MOS transistors for optimum operation. The implementation of full adder with 8 MOS transistors is shown in fig. 5. Fig. 10 and Fig. 11 represent the layout optimization and simulation waveforms respectively.

c) Proposed full adder:-3

Another technique for full adder implementation is proposed with 9 MOS transistors. The logical expressions in Eq. (1) and Eq. (2) can be implemented with 3 transistor XOR circuit or 3 transistor XNOR circuit, an inverter and a 2:1Mux as shown in fig. 6 and fig. 7. Fig. 12 and Fig. 13 represent the layout optimization and simulation waveforms of 9 transistor full adder respectively. Simulation was carried out with supply voltage scaling from 1.2V to 0.6V &0.6V to 0.3V. The transistors with low threshold voltage at critical paths of the circuits and high threshold voltage at Non critical paths were used to obtain optimized power dissipation & delay.

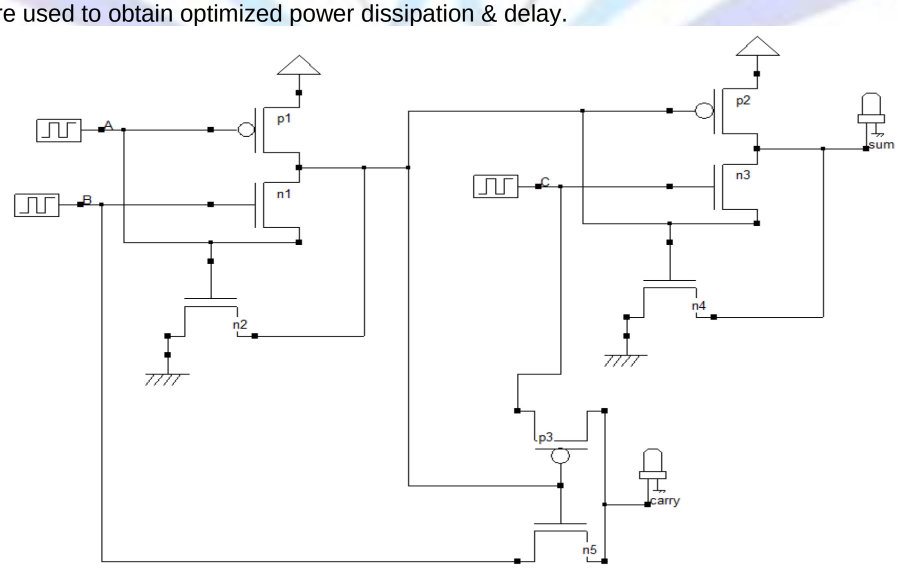

Fig. 5Full adder implementation with 8 MOS transistors

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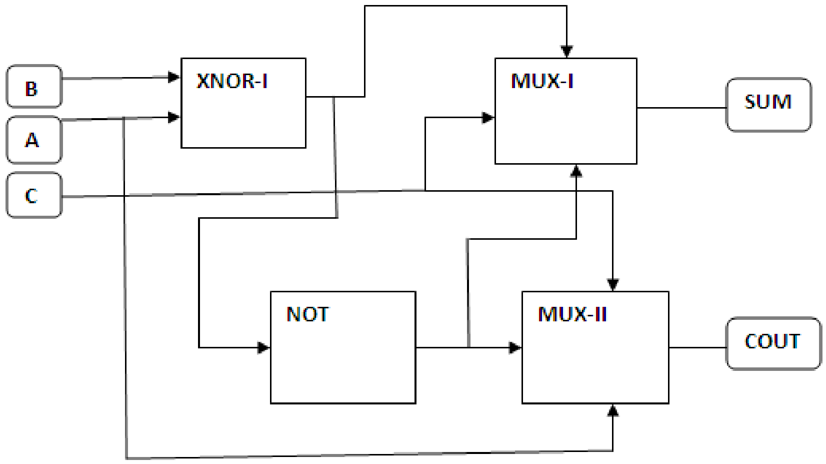

Fig. 6 Structure of Full adder with 9 transistors

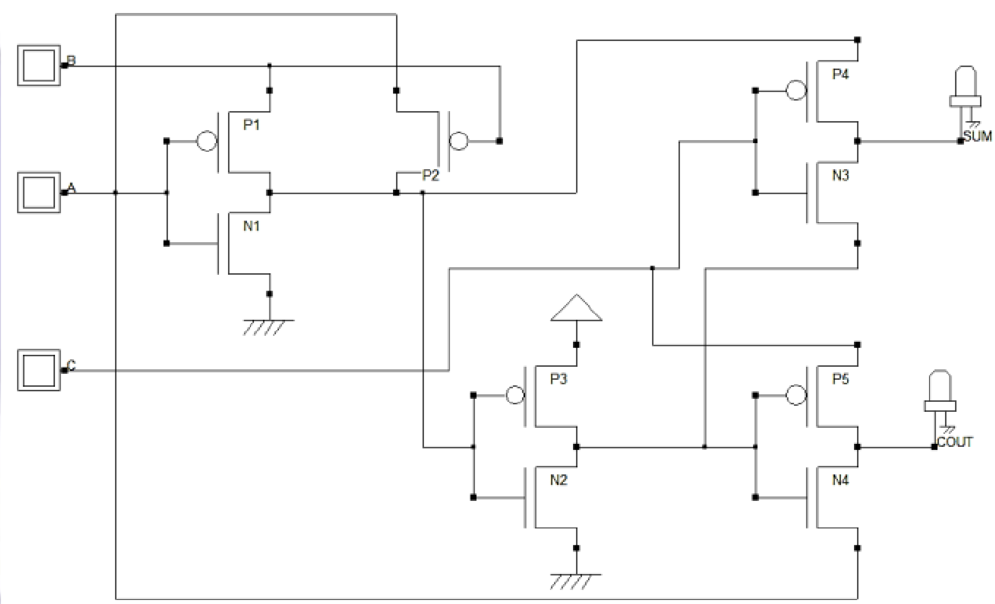

Fig. 7 Full adder implementation with 9 MOS transistors

4. PERFORMANCE ANALYSIS AND SIMULATION RESULTS.

The simulations were performed with supply voltage V_{DD} scaling from 1.2V to 0.6V&0.6V to 0.3V, using 90 Nanometer (nm) Micro wind 3 CMOS layout CAD Tool. The performance was analyzed in terms of delay, power dissipation, power delay product, area and compared with existing techniques. The results are shown in Table 2, Table 3 and Table 4, they indicate good improvement in power, delay and area, which dictates the efficiency the proposed techniques.

Table 2 Performance Analysis of Layout

Parameter	Reference Paper [10]	Proposed work 1	Proposed work 2	Proposed work 3
Number of MOS Transistors	11	10	8	9
$V_{DD}1$=1.2V, $V_{DD}2$=1.2V Power (µw)	61.269	1.819	111.2	11.83

High Threshold voltage(V_{th}) Power (μw)	---	1.642	137	11.82
Delay(ns)	1.380	0.21	1	0.25
PDP(femito), V_{DD}=1.2V	84.55	0.38	111	2.9
$V_{DD}1$=1.2V, $V_{DD}2$=0.6V Power (μw)	---	1.697	110	11.76
$V_{DD}1$=0.6V, $V_{DD}2$=0.3V Power (μw)	---	0.867	33	0.427
Area(μm^2)	235	260	84	29
Point A				
C	7.10	8.37	7.10	1.52
MC	2.53	2.53	2.5	0.58
CC	0.01	0.01	0.00	0.00
DC	0.07	0.53	0.38	0.12
GC	4.50	5.31	4.15	0.82
Point B				
C	9.88	5.6	7.10	0.54
MC	5.41	0.55	2.5	0.20
CC	0.04	0.01	0.00	0.00
DC	0.20	0.26	0.38	0.03
GC	4.28	4.87	4.15	0.31
Point C				
C	20.56	7.2	2.02	1.20
MC	4.97	2.32	0.51	0.27
CC	0.03	0.01	0.00	0.00
DC	0.13	0.42	0.20	0.03
GC	15.46	5.01	1.31	0.90
Carry				
C	4.63	1.57	1.21	1.20
MC	4.40	1.14	0.74	0.27
CC	0.02	0.00	0.00	0.00
DC	0.23	0.43	0.47	0.03
GC	0.00	0.00	0.00	0.90
Sum				
C	4.88	3.0	1.72	0.37
MC	4.69	2.3	1.29	0.29
CC	0.01	0.01	0.00	0.00
DC	0.20	0.70	0.43	0.08
GC	0.00	0.00	0.00	0.00

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Table 3 Performance Analysis of schematic circuits

Full Adders	Delay (ns)	Power Dissipation(µw)	Power delay product (Femito)	Area (µm^2)
10 Fa High Vt	1.260	17.53	22	308
10 Fa Low Vt	1.110	11.54	12	252
10 Fa High & Low Vt	1.170	17.53	21	315
9 Fa High Vt	1.730	9.72	16	253
9 Fa Low Vt	0.860	9.62	9	234
9 Fa High & Low Vt	1.600	10.14.	15.6	258
8 Fa High Vt	1.020	226	230	256
8 Fa Low Vt	0.890	191	171	204
8 Fa High & Low Vt	0.880	182	160	192

Table 4 Performance Analysis of Schematic Circuits

	Proposed work 1	Proposed work 2	Proposed work 3
Power (µw) VDD1=1.2V,VDD2=0.6V	4.027	3.422	132
Power (µw) VDD1=0,6V,VDD2=0.3V	1.152	3.20	3.422
Area (µm^2)	287	210	174

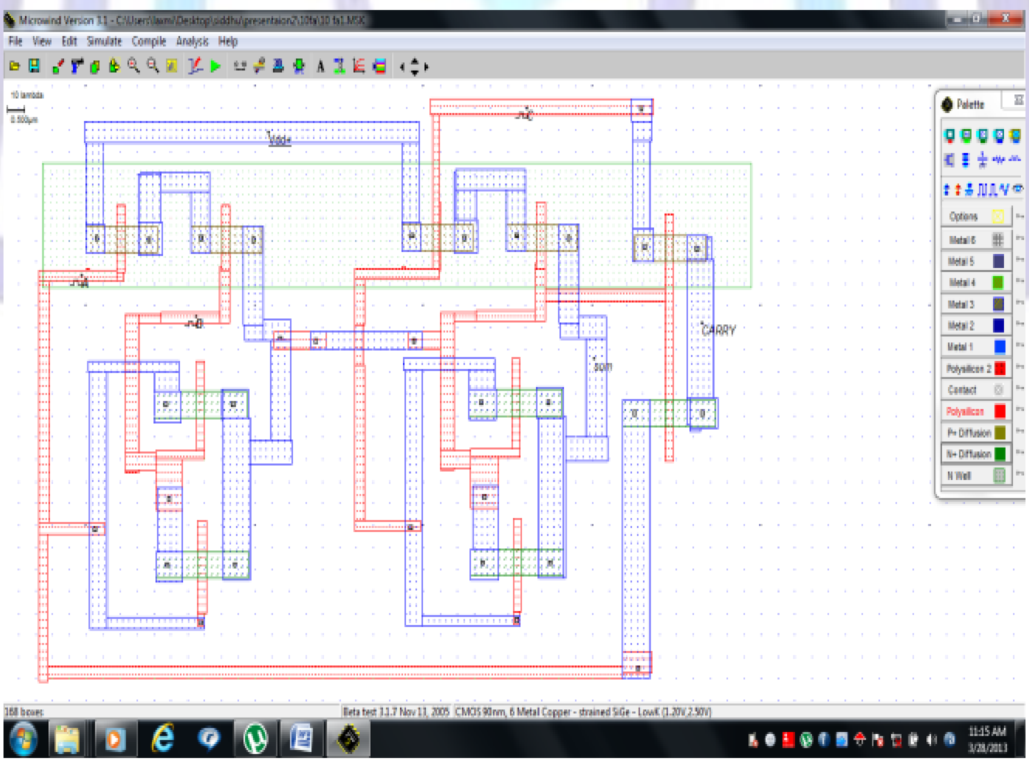

Fig. 8 Layout optimization for proposal 1

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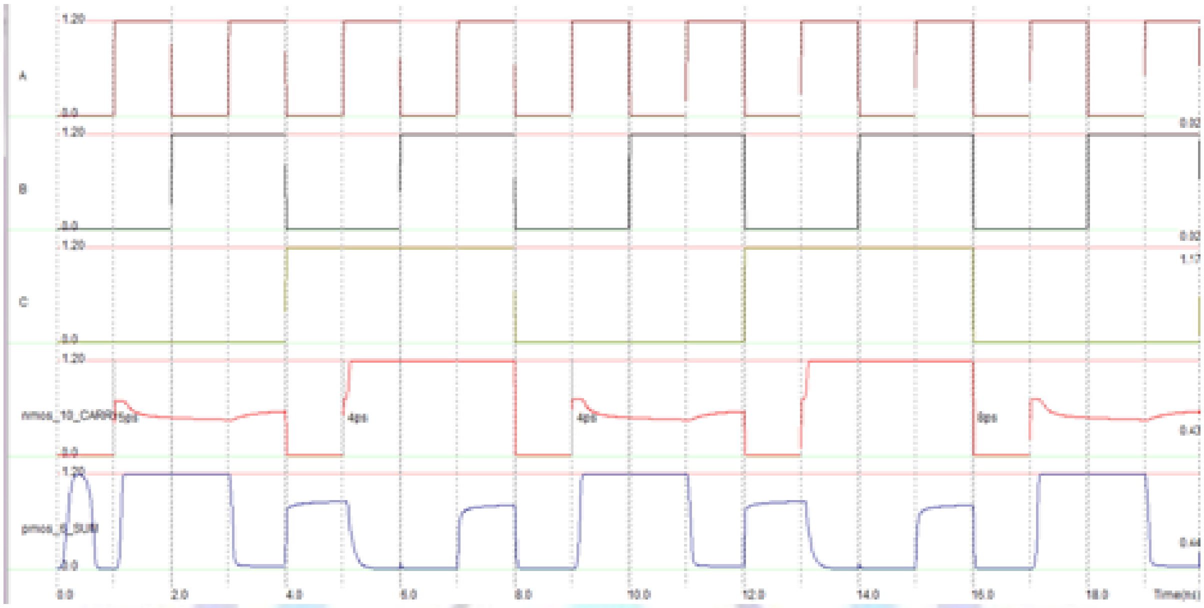

Fig. 9 Simulation results for proposal 1

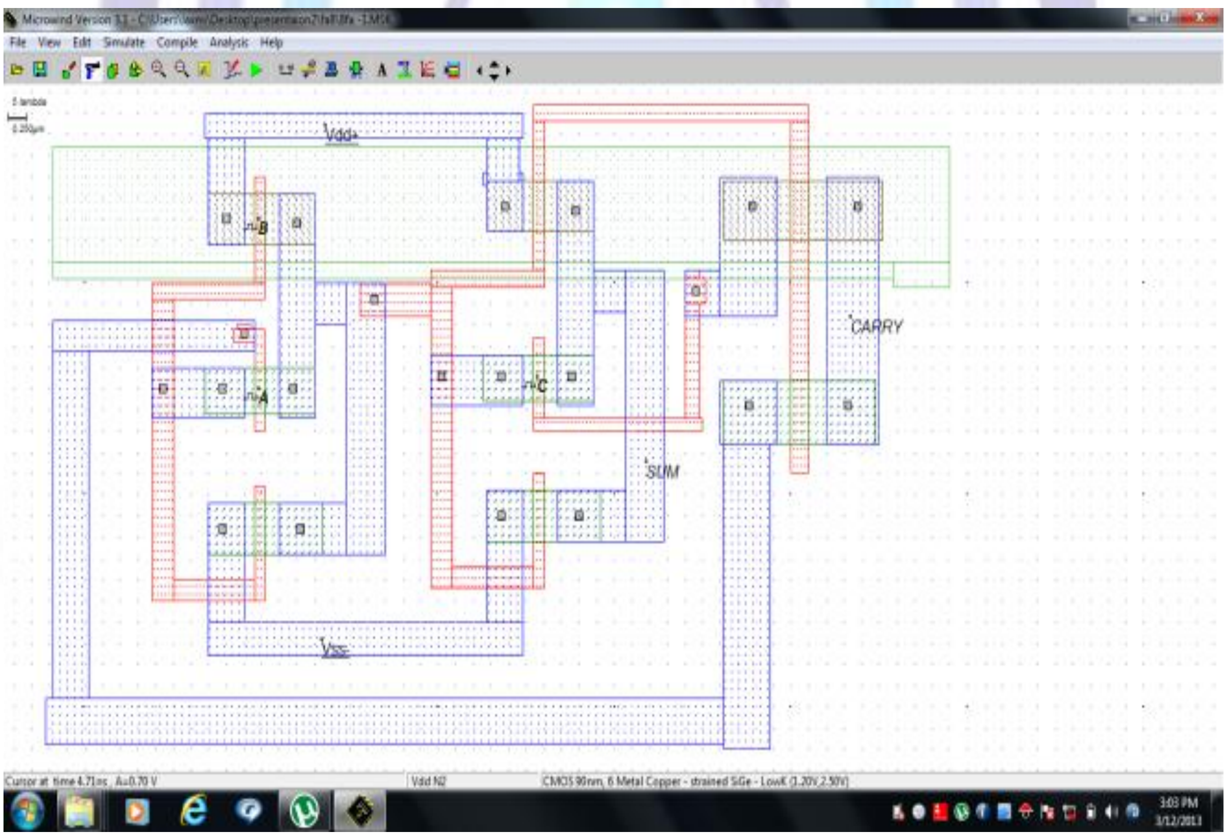

Fig. 10 Layout optimization for proposal 2

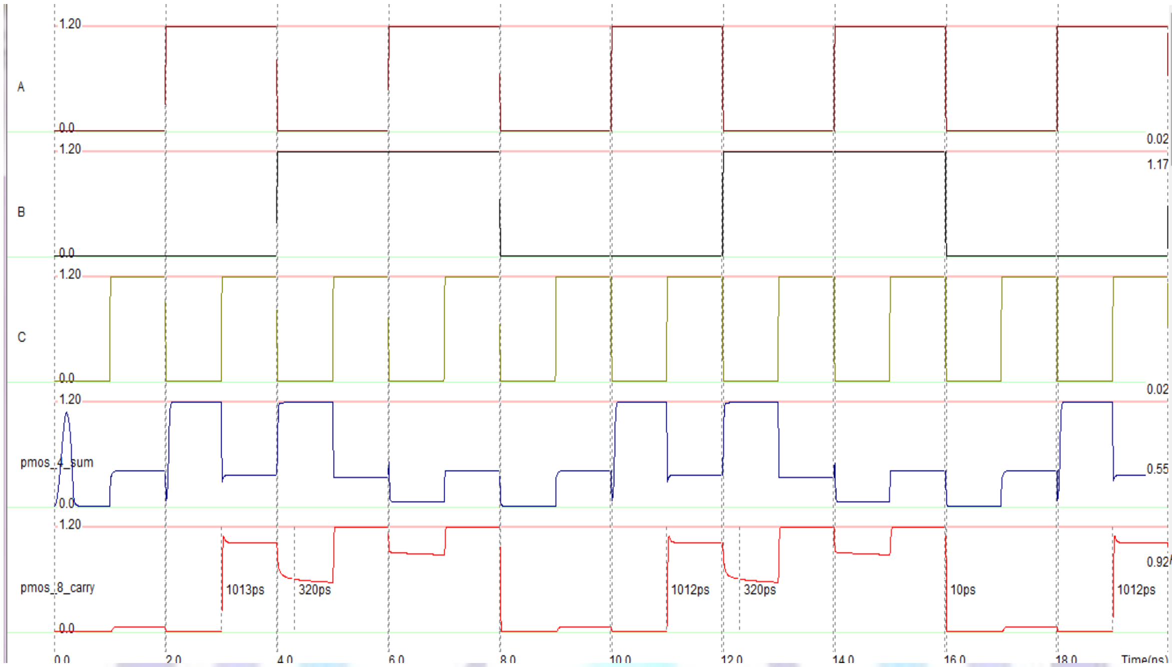

Fig. 11 Simulation results for proposal 2

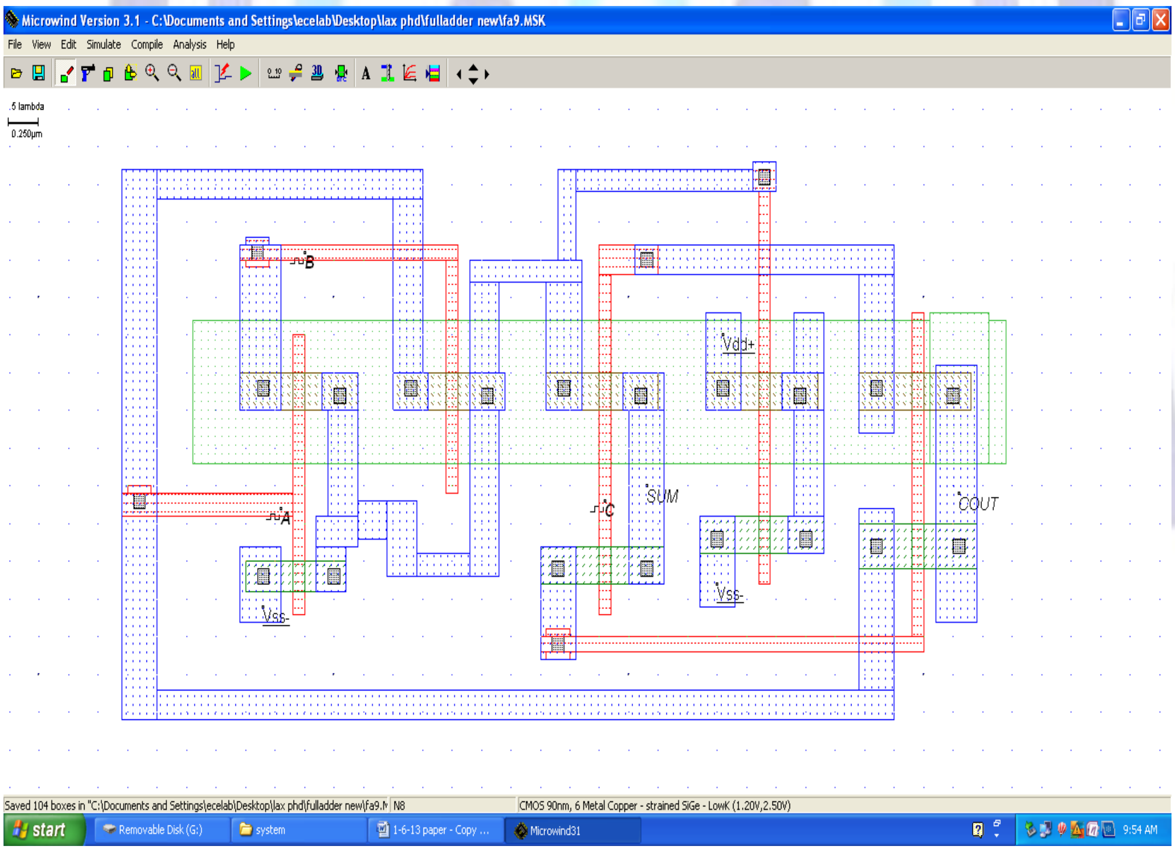

Fig. 12 Layout optimization for proposal 3

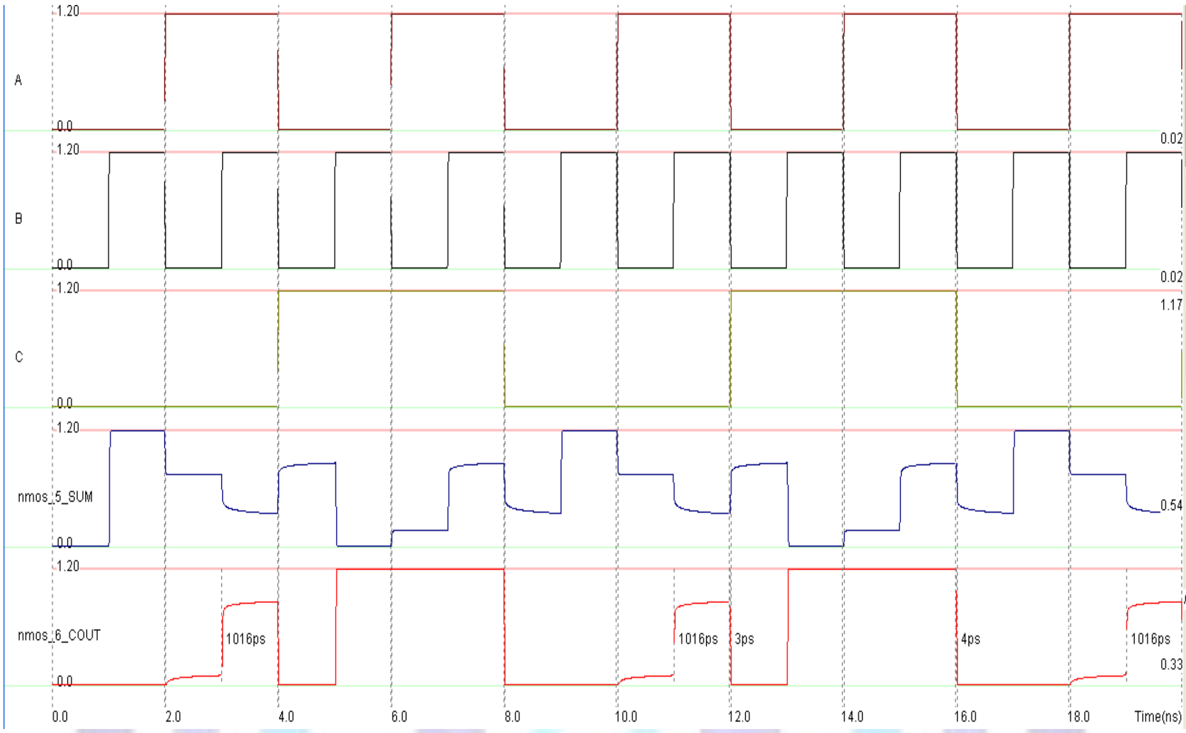

Fig. 13 Simulation results for proposal 3

5. CONCLUSIONS

The present paper demonstrated the improvement in parameters Viz. area, power, delay and capacitances with reduction in number of transistors to implement Full adder circuits. The design architecture shows good reduction in area, power consumption. The simulations were performed using 90nm Micro wind 3 CMOS layout CAD Tool. The performance of ALU improves by incorporating the proposed technique for adders in it. Still the performance of Full adder can be improved by incorporating techniques which support reduced transistor implementations.

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