



Microprocessor Architecture Era for Development Cloud Computing of Ministry of Electricity and Energy of Egypt

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ABSTRACT

A development and evaluation the Cloud Computing (CIComp) of Ministry of Electricity and Energy of Egypt (MEEE) is presented in this paper. In order to be able to judge whether the CIComp of MEEE is competence, there is a need to develop criteria which performance can be judged. Competency based standards and the ability to perform the activities within an occupation to the standard expected in the organization structure are presented. The key objective of Cloud Computing is to integrate Authorized Groups (AuthGs) development with the needs of the organization structures of MEEE. The CIComp of MEEE was developed jointly between the telecommunication information technology and CIComp services. Evaluation enables participant to distinguish between AuthGs centered view and a customer centered view of cloud computing of MEEE is competence evaluation. Recognize the main types of evaluation, explain the purpose of evaluation compare the approaches to cloud computing evaluation and review the relationship between the process and policy of evaluation are investigated. Microprocessor architecture presented an optimistic view of multicore scalability to develop the CIComp. Moreover this paper investigates the theoretical analysis of multiprocessor developing and scalability. The analysis was based on the laws of Amdahl's, Gustafson's, Hill's and Marty for fixed-workload condition. Moreover, challenged the difficulties to develop better cloud computing is taken into account. Also, multicore analysis of CIComp scalability, performance and power under fixed-time and memory-bound conditions are studied. These results complement existing studies and demonstrate that CIComp architectures are capable of extensive scalability and developing.

Indexing terms/Keywords:

CIComp; MEEE; AuthGs; Parallelization and Microprocessors.

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I. INTRODUCTION

The CComp advancements in communication technology and significant growth in the wireless communication market and consumer demands demonstrate the needs for the organization structure of MEEE, more reliable and power efficient, integrated wireless system. Cloud computing has the benefits of cost reduction and improving system reliability. CComp is considered to be the important components of integrated internet wireless systems [1-10]. The new CComp network architecture of MEEE consists of: information centric networking, CComp integrated with networking, and the link networks. CComp of MEEE networking offers a unique combination and integration of cloud computing and virtual networking. CComp provides services to the customers from the data center hardware and software. The applications delivered as services over the Internet, the hardware and systems software in the datacenters which allow those services. Data center hardware and software that will call the CComp. It is a solution that distributes the benefits of CComp more deeply into the network, and provides a more compact integration of virtualization features at cloud computing and networking levels.

There are main factors for the design and implementation of Cloud Computing [11-13]. Early studies have shown that performance of the CComp such as efficiency and energy requirements increase, while the cost decrease. The fundamental of the theoretical study introduced by Amdahl's law [14], later reexamined by Gustafson's, Hill's and Marty [15, 16] related to the microprocessor with its performance. While, the CComp of MEEE has its own conceptual, technical, economic and AuthGs experience characteristics. The service oriented, loose coupling, strong fault tolerant, business model and ease use are main characteristics of CComp of MEEE. Clear insights into CComp of MEEE will help the development and adoption of this evolving technology both for academe and industry.

Theremained of thispaper is organized as follows: Section II provides the organization structure of MEEE. Section III discusses the developing and evaluating CComp of MEEE. Section IV shows qualitative and quantitative collection procedures of CComp of MEEE network. Section V introduces the basic concepts of CComp of MEEE. Section VI discusses the results and comparison. Finally, the entire work is summarized in section VII.

II. ORGANIZATION STRUCTURE of MEEE

It is necessary to plan the organizational structure of MEEE before construct the CComp in a way that maximizes performance, power, energy, efficiency and profitability. Fig. 1 shows the organizational structure of MEEE. All of the duties and responsibilities of those in the MEEE structure must be identified. Lines of authority must be carefully delineated, so that all members of the organization will understand what their job responsibilities are. The study has been made for every function, so that CComp of MEEE must be organized in such a way that best serves its needs and makes the business a success.

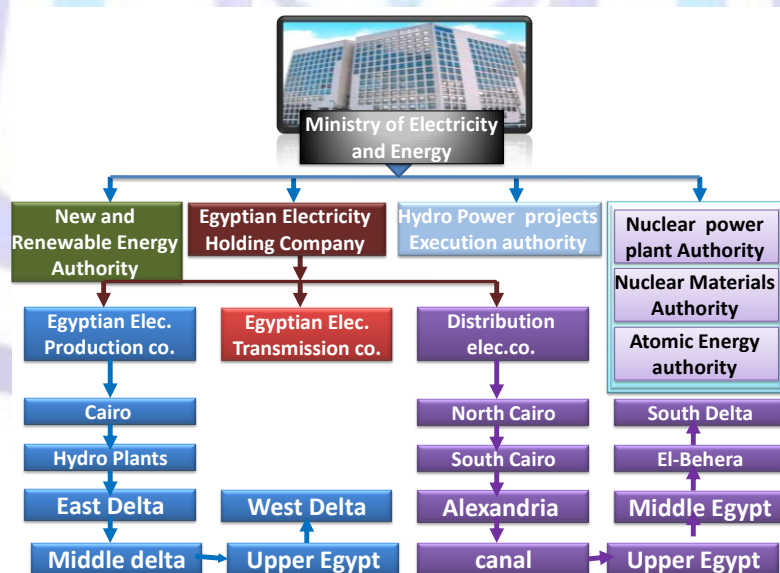


Fig. 1: The organizational structure of Egyptian Ministry of Energy and Electricity.

III. DEVELOPING AND EVALUATING CLOUD COMPUTING OF MEEE

The development of MEEE is a subject of wider field of utilizing and employing CComp since at its core is the question of how the AuthGs in the workplace. In order to achieve this aim, MEEE have adapted a process which take into account both development and above stated basic principles. Content of the CComp of MEEE includes an analysis of such issues as award restructuring, multiskilling, broadbanding and career path development. It also develops knowledge and skills which enable workplace to be implements. Specifically in terms of job performance in the organization, it can be summarized as being the discrepancy between the current performance and ideal performance. The aim is to provide the AuthGs of MEEE the knowledge, skills and abilities to undertake three areas of MEEE job, needs analysis, network and package program design and evaluation.



IV. QUALITATIVE AND QUANTITATIVE COLLECTION PROCEDURES OF CLOUD COMPUTING OF MEEE NETWORK

The array of collection devices outlined can be conveniently divided into qualitative and quantitative collection procedures. Quantitative procedures usually require numerical analysis, while qualitative procedures are more subjective and it to do with making judgment about the value of something, both have their place in evaluation. Evaluation is the process of delineating and providing descriptive and judgmental information about the worth and merit of CIComp of MEEE Network goals, design, implementation and impact in order to guide decision making, service needs for accountability and promote understanding of process.

V. BASIC CONCEPTS OF CLOUD COMPUTING OF MEEE

The basic concepts of CIComp of MEEE shows in Fig. 2. The voltage transducer takes an analog voltage signal from a 220V wall outlet and converts it to acceptable levels. The low pass filter eliminates the high frequency components, and the analog to digital converter transforms the analog signal into digital data. A microprocessor is used to generate the sampling pulses synchronized to the one-pulse-per-second (1PPS) timing signals from the Global Positioning System (GPS) receiver integrated into the Frequency Disturbance Recorder Structure (FDRS). The FDRS makes frequency calculations using algorithms of phasor analysis and signal re-sampling techniques. The complexity of the calculations is minimized to allow the microprocessor time to complete its other tasks and prevent data overflow. The phase angle, frequency, and rate of frequency change are computed using phasor techniques developed specifically for single phase measurements. The computed values are time stamped, and transferred to the Information Management System (IMS) via the Satellite, Internet and mobile telephone.

After receiving the data from the FDRS, the IMS server processes, time aligns, saves it in a database and provides data for the web service to display the information online. CIComp provides the integrated wide area communication media between FDRS and IMS server. The IMS is made up of three main components: the application server program, which is used to receive the frequency data from the FDRS; the database operation service, which is used to store all the data into a database and provide for frequency analysis; web service, which is used to provide an interface for the users, such as our customers and partners, who want to observe the frequency information from anywhere on the Internet. The IMS is a vital component in the Frequency Monitoring Network Server Program (FMNSP) system. It is based on multitier customer/server architecture. The IMS models, coordinates, and integrates the frequency acquisition, processing and display functions. The IMS server controls data communication and database operation transactions and asynchronous queuing to ensure reliable completion of all the transactions. It also provides access to resources based on names instead of locations and, thereby, improves scalability and flexibility as system components are added or moved.

Rapid advances in networking and CIComp technologies have fueled the emergence of the "Web Service" model for enterprise computing. Successful examples of commercially viable Web services include Service Provider and AuthGs. Database as a Service model provides users power to create, store, modify, and retrieve data from anywhere in the world, as long as they have access to the CIComp. It introduces several challenges, an important issue being data privacy. It is in this context that can be specifically address the issue of data privacy. There are two main privacy issues. First, the owner of the data needs to be assured that the data stored on the service-provider site is protected against data thefts from outsiders. Second, data needs to be protected even from the service providers, if the providers themselves cannot be trusted. The strategy is to process as much of the query as possible at the service providers' site, without having to decrypt the data. Decryption and the remainder of the query processing are performed at the client site and explore an algebraic framework to split the query to minimize the computation at the client site. After Web Service receiving the data from the costumer or AuthGs, the IMS server processes, time aligns, saves it in a database and provides data for the web service to display the information online to serve the costumer.

A group working system includes a plurality of work stations interconnected through a network and each having a multi-window function. Each work station is provided with a group working user interface program executed under the control for transferring control information for a group work. When input operation is performed for a window of a group working mode in any one of the work stations, indication information for identifying an operator performing the input operation is output to an additional window which is paired with the above-mentioned window. By making reference to the indication information, each user can avoid conflict in the input operation to the same window of the group working mode with other users. The market is considered supply function equilibrium model of interaction in an electricity market. Market is assuming a linear demand function and considers a competitive fringe and several strategic players having capacity limits and affine marginal costs. After Web Service receiving the data from the operation, the IMS server processes, time aligns, saves it in a database and provides data for the web service to display the information online to serve the workers of each of the following Generators or Transmission or Distribution or costumers.

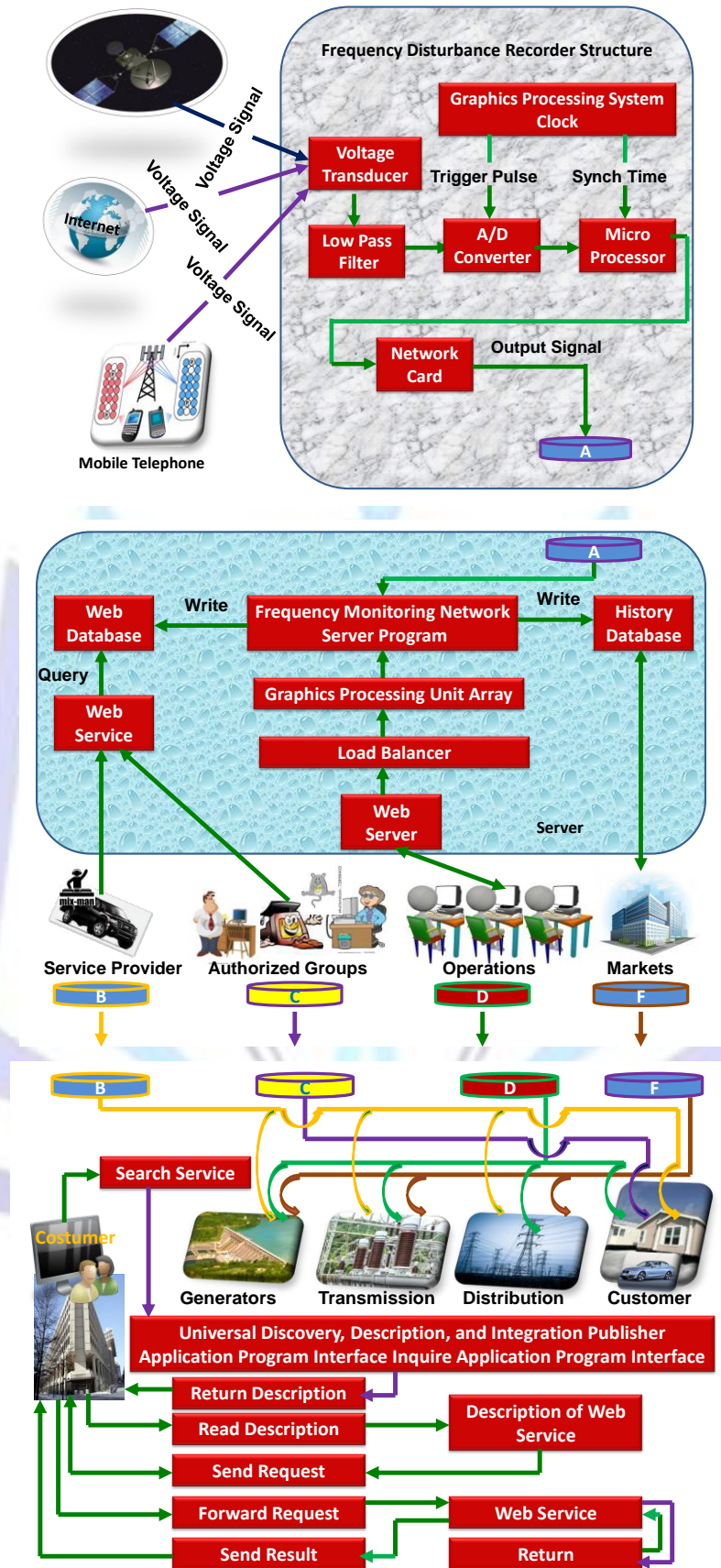


Fig. 2: Basic Concepts of CiComp of MEEE.

A central broker must be available that allows implementers to register their services as well as costumers to locate these services. Universal Discovery, Description, and Integration see all functionality expected from a service



broker. Servers use the Publishers Application Program Interface to register services as well as additional business information with the global repository. Costumers access the Inquiry Application Program Interface to browse the repository and retrieve service descriptions. Simple Object Access Protocol is used as communication protocol in all interactions. The client obtains the Web Services Description Language description from the Universal Discovery, Description, and Integration repository both dynamically or statically, generates a client-side proxy, and invokes the Web service.

VI. REQUIREMENT OF CLOUD COMPUTING DESIGN

A) Develop Analytical Power, Energy Efficiency and Performance Models

1) Models of Symmetric Many-core Processor that Replicates a State of the Art Superscalar Processor on a Die:

Efficiency is usually defined as price per performance:

$$\eta(S_{up}, N_p) = \frac{S_{up}(\varphi, N_p)}{N_p} \tag{1}$$

High efficiency means that the use of devices effectively. Low efficiency means that resources are wasted.

According to Amdahl's law [17-19], the formula for computing the theoretical maximum speedup $S_{up}(\varphi, N_p)$ (or performance) achievable through parallelization is as follows:

$$S_{up}(\varphi, N_p) = \frac{1}{\varphi + \frac{(1-\varphi)}{N_p}} \tag{2}$$

where N_p is the number of processors, and φ is the fraction of computation that programmers can parallelize ($0 \leq \varphi \leq 1$). To model the power consumption for a θ many-core processor, new variable θ is introduced, to represent the fraction of power the processor consumes in idle state ($0 \leq \theta \leq 1$). Assume that one superscalar processor in active state consumes a power of 1. By definition, the amount of power one full-blown processor consumes during the sequential computation phase is 1, while the remaining $(N_p - 1)$ full-blown processors consume $(N_p - 1)\theta$. Thus, during the sequential computation phase, θ consumes $1 + (N_p - 1)\theta$. For the parallel computation phase, N_p full-blown processors consume N_p amount of power. Because it takes $(1 - \varphi)$ and φ/N_p to execute the sequential and parallel code, respectively, the formula for average power consumption denoted by $P_{AvPowCon}$ for a Ψ is as follows [20]:

$$P_{AvPowCon}(\varphi, N_p, \theta) = \frac{(1-\varphi)[1 + (N_p - 1)\theta] + \frac{\varphi}{N_p}}{1 + \varphi(N_p - 1)} \tag{3}$$

$$P_{AvPowCon}(\varphi, N_p, \theta) = \frac{1 + (N_p - 1)\theta(1-\varphi)}{1 + \varphi(N_p - 1)} \tag{4}$$

Where; $\beta_{perf}(\varphi, N_p) = \frac{1}{1 + \varphi(N_p - 1)}$ (5)

Now, we can model $(\beta_{perf}(\varphi, N_p) / P_{AvPowCon}(\varphi, N_p, \theta))$ to the *performance per watt* $(\beta_{perf}(\varphi, N_p) / W)$, which represents the performance achievable at the same cooling capacity, based on the average power $(P_{AvPowCon}(\varphi, N_p, \theta))$. This metric is essentially the reciprocal of energy, because the definition of performance is the reciprocal of execution time. Because $(\beta_{perf} / P_{AvPowCon})$ of single-core execution is 1, the $(\beta_{perf}(\varphi, N_p) / P_{AvPowCon}(\varphi, N_p, \theta))$ benefit of a θ is expressed as:

$$\frac{\beta_{perf}(\varphi, N_p)}{P_{AvPowCon}(\varphi, N_p, \theta)} = (\varphi, N_p, \theta) = \frac{1}{1 + \varphi(N_p - 1)} \cdot \frac{1 + \varphi(N_p - 1)}{1 + (N_p - 1)\theta(1-\varphi)} \tag{6}$$

$$(\varphi, N_p, \theta) = \frac{1}{1 + (N_p - 1)\theta(1-\varphi)} \tag{7}$$

In addition to $(\beta_{perf}(\varphi, N_p) / P_{AvPowCon}(\varphi, N_p, \theta))$, *performance per joule* $(\beta_{perf}(\varphi, N_p) / \text{Joule})$ can also model *per joule*, a metric for evaluating the performance achievable in the same battery life cycle or, more specifically, energy. $\beta_{perf}(\varphi, N_p) / \text{Joule}$ is equivalent to the reciprocal of energy-delay product. The formula for performance per joule is as follows:

$$\frac{\beta_{perf}(\varphi, N_p)}{\text{Joule}} = \frac{\beta_{perf}(\varphi, N_p)}{J(\varphi, N_p, \theta)} = (\varphi, N_p, \theta) \tag{8}$$



$$(\varphi, N_p, \theta) = \frac{1}{(1 + \varphi(N_p - 1))(1 + (N_p - 1)\theta(1 - \varphi))} \tag{9}$$

2) Models of Symmetric Many-core Processor that Replicates a Smaller, More Power Efficient Core on a Die:

The performance model of V many-core processor has been considered. This model assumes that one larger core consumes the same amount of die area that several smaller cores consume. We slightly modified this performance model to accommodate arbitrarily sized cores. To model the performance difference between a full-blown processor (N_p) and an efficient core (V), we introduce the variable v . This variable represents an efficient core's performance normalized to that of a full-blown processor ($0 \leq v \leq 1$). Because each efficient core's performance is sc , the formula for calculating V 's performance model is as follows:

$$\beta_{perf}(\varphi, N_p, v) = \frac{v}{(1 - \varphi) + \frac{\varphi}{N_p}} \tag{10}$$

To model V 's power consumption, we need two new variables: v and θ_v . The first variable represents an active efficient core's power consumption relative to that of an active full-blown processor ($0 \leq v \leq 1$); the second represents the fraction of an efficient core's idle power normalized to the same core's overall power consumption ($0 \leq v \leq 1$). During the sequential computation phase, one efficient core in active state consumes v , and all idle cores consume $(N_p - 1)v\theta_v$. During the parallel computation phase, all efficient cores consume $N_p v$. Because it takes $(1 - \varphi)/v$ and $N_p / (N_p \times v)$ to perform sequential and parallel computation, respectively, the average power consumption by a V is:

$$P_{AvgPowCon}(\varphi, N_p, \theta_v, v, v) = \frac{\frac{(1 - \varphi)[1 + (N_p - 1)v\theta_v] + \frac{\varphi}{N_p}v}{v}}{\frac{(1 - \varphi) + \frac{\varphi}{N_p}}{v}} \tag{11}$$

$$P_{AvgPowCon}(\varphi, N_p, \theta_v, v, v) = \frac{v + (N_p - 1)v\theta_v(1 - \varphi)}{(1 - \varphi) + \frac{\varphi}{N_p}} \tag{12}$$

Thus, the following equations can represent $(\varphi, N_p, \theta_v, v, v)$ and $(\varphi, N_p, \theta_v, v, v)$:

$$(\varphi, N_p, \theta_v, v, v) = \frac{v}{v + (N_p - 1)v\theta_v(1 - \varphi)} \tag{13}$$

$$(\varphi, N_p, \theta_v, v, v) = \frac{v}{(1 - \varphi) + \frac{\varphi}{N_p}} \cdot \frac{v}{v + (N_p - 1)v\theta_v(1 - \varphi)} \tag{14}$$

3) Models of Asymmetric Many-core processor with Numerous Efficient Cores and one Bull-blown Processor as the Host Processor:

The performance model of a $\theta + V$ studies for many-core processor. Executing the sequential code at the host processor N_p takes $(1 - \varphi)$, whereas executing the parallel code using the efficient cores takes $\varphi / ((N_p - 1)v)$. A $\theta + V$ many-core processor contains one N_p and $(N_p - 1)V$ cores. Note that we assume the host processor to be idle while the efficient cores are executing the parallel code. Thus, the formula for computing performance improvement using a $\theta + V$ is as follows:

$$\beta_{perf}(\varphi, N_p, v) = \frac{v}{(1 - \varphi) + \frac{\varphi}{(N_p - 1)v}} \tag{15}$$

During the sequential computation phase, the amount of power the full-blown processor consumes is 1, and the amount the efficient cores consume is $(N_p - 1)v\theta_v$. During the parallel computation phase, its full-blown processor consumes θ ,



while the efficient cores consume $(N_p - 1)V$. Because executing sequential and parallel code takes $(N_p - 1)$ and $\varphi/(N_p - 1)V$ the average power is:

$$P_{AvPowCon}(\varphi, N_p, \theta_{V,V,V}) = \frac{(1-\varphi)[1 + (N_p - 1)\gamma\theta_V] + \frac{\varphi}{V} \left(\frac{\theta}{N_p - 1} + V \right)}{(1-\varphi) + \frac{\varphi}{(N_p - 1)V}} \quad (16)$$

Consequently, $(\varphi, N_p, \theta_{V,V,V})$ of a $\theta + V$ is expressed as:

$$(\varphi, N_p, \theta_{V,V,V}) = \frac{1}{(1-\varphi)[1 + (N_p - 1)\gamma\theta_V] + \frac{\varphi}{V} \left(\frac{\theta}{N_p - 1} + V \right)} \quad (17)$$

and $(\varphi, N_p, \theta_{V,V,V})$ of a $\theta + V$ as:

$$(\varphi, N_p, \theta_{V,V,V}) = \frac{V}{(1-\varphi) + \frac{\varphi}{(N_p - 1)V}} \cdot \frac{1}{(1-\varphi)[1 + (N_p - 1)\gamma\theta_V] + \frac{\varphi}{V} \left(\frac{\theta}{N_p - 1} + V \right)} \quad (18)$$

VII. RESULTS DISCUSSION

The Graphical User Interface (GUI) is evaluating the CIComp of MEEEas shown in Fig. 3. The aim of this study is to improve the performance of cloud computing and programming model to be very successful. This section will compare different performance of multi-core including the different formula of speedup for cloud computing. The outline the basic requirements of a multi-core for cloud computing and analyze each of the compared multicore processors under that guideline.

The efficiency of fixed size speedup is calculated under different framework scenarios of the portion of the workload that can be parallelized and the number of processors, as shown in Fig. 4-(a). Although it is true that lower workload that can be parallelized and the number of processors a many-core system will deliver higher compute throughput than a multi-core system. The average power consumption (superscalar processors) is shown in Fig. 4-(b). The horizontal axis represents the number of processors (cores), scaled from 1 to 1024.

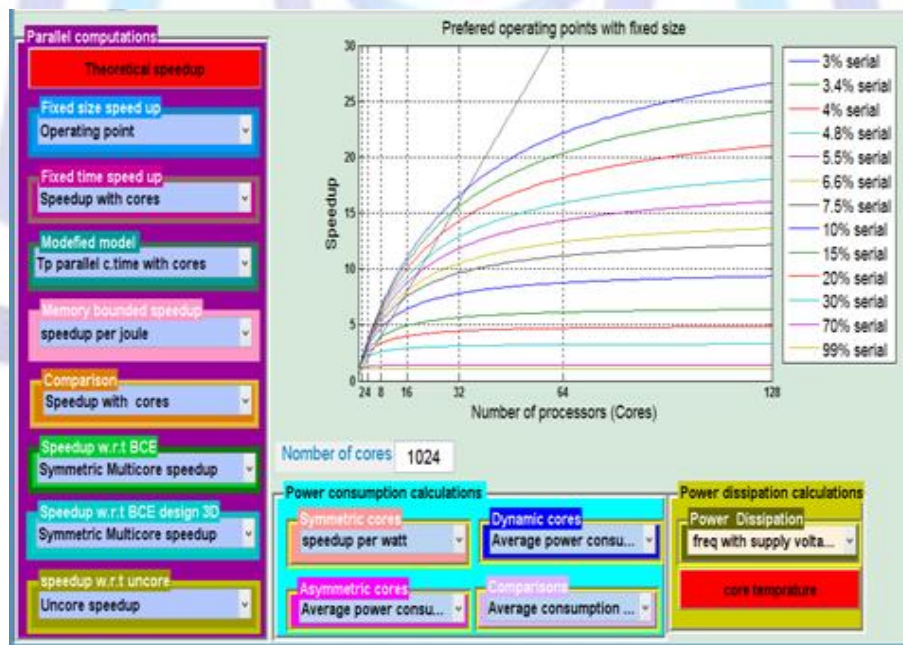


Fig. 3: GUI Model of CIComp of MEEE.

The vertical axis represents the average power consumption (superscalar processors). The average power consumption is calculated in accordance with different framework scenarios of the portion of the workload. If the number of processors a many-core system will deliver higher compute throughput than a multicore system, the average power consumption is higher

The model is efficient core's power consumption as one-fourth that of a full-blown processor. When the efficient core's performance to be one-half that of a full-blown processor and its fraction of power to be 25 percent. Fig. 4-(c) shows



the speedup per Watt when the number of cores is varied from 1 to 1024, To model ∇ power consumption and executing the sequential code at the host processor θ . This happens mainly because the performance to power ratio of an efficient core is better than that of a full blown processor. As the number of cores increases, the amount of energy consumption becomes higher than that of a single core full blown processor baseline. Moreover, Fig. 4-(d) shows that Performance per Joule of a power consumption. However, if the application is embarrassingly parallel that is, it has high the portion of the workload values. This means that performance saturation is the main contributor that leads to a reduction performance per joule.

From the speedup factors, the efficiencies for the various numbers of processors are easily determined. Fig. 5.(a) shows that the relative average efficiency steadily decreases as more hosts are added to the virtual machine. Execution time is not always the most convenient metric by which to evaluate parallel algorithm performance. As execution time tends to vary with problem size, execution times must be normalized when comparing algorithm performance at different problem sizes. Efficiency the fraction of time those processors spend doing useful work is a related measure that can sometimes provide a more convenient measure of parallel algorithm quality. It characterizes the effectiveness with which an algorithm uses the computational resources of a parallel computer in a way that is independent of problem size. As the speedup factor approaches its asymptote, the efficiency plummets. This means that small gains in speed come at the cost of inefficient multi-core use. Working multi-core of cloud computing consumed much more energy. Because the reaction releases energy much more quickly, it delivers far more power with the number of processors. If the parallel and serial time is the amount of work performed during a period of time of duration, the average power over that period is given by with variation of number of processors can be seen in Fig. 5-(b).

Power realizes multi-core processors in various power modes to reduce energy consumption with a corresponding decrease in peak speedup of multi-core processor. Fig. 5-(c) has shown performance per power realized clusters can conserve significant energy with minimal performance loss running parallel multicore. Such savings are typically achieved using a priori knowledge of application performance. Accurate prediction of parallel power consumption and performance is an open problem. Performance per joule can model, a measure for evaluating the performance achievable in the same battery life cycle or, more specifically, energy. Performance per joule is equivalent to the reciprocal of energy-delay product. The behavioral analysis of the performance per joule for scalability issue in multi-core is concluded as shown in Fig. 5-(d). Simulation results show that value of performance per joule under different framework scenarios of the portion of the workload that can be parallelized and the number of processors, the results in ranges from 10% to 99.9% decreases.

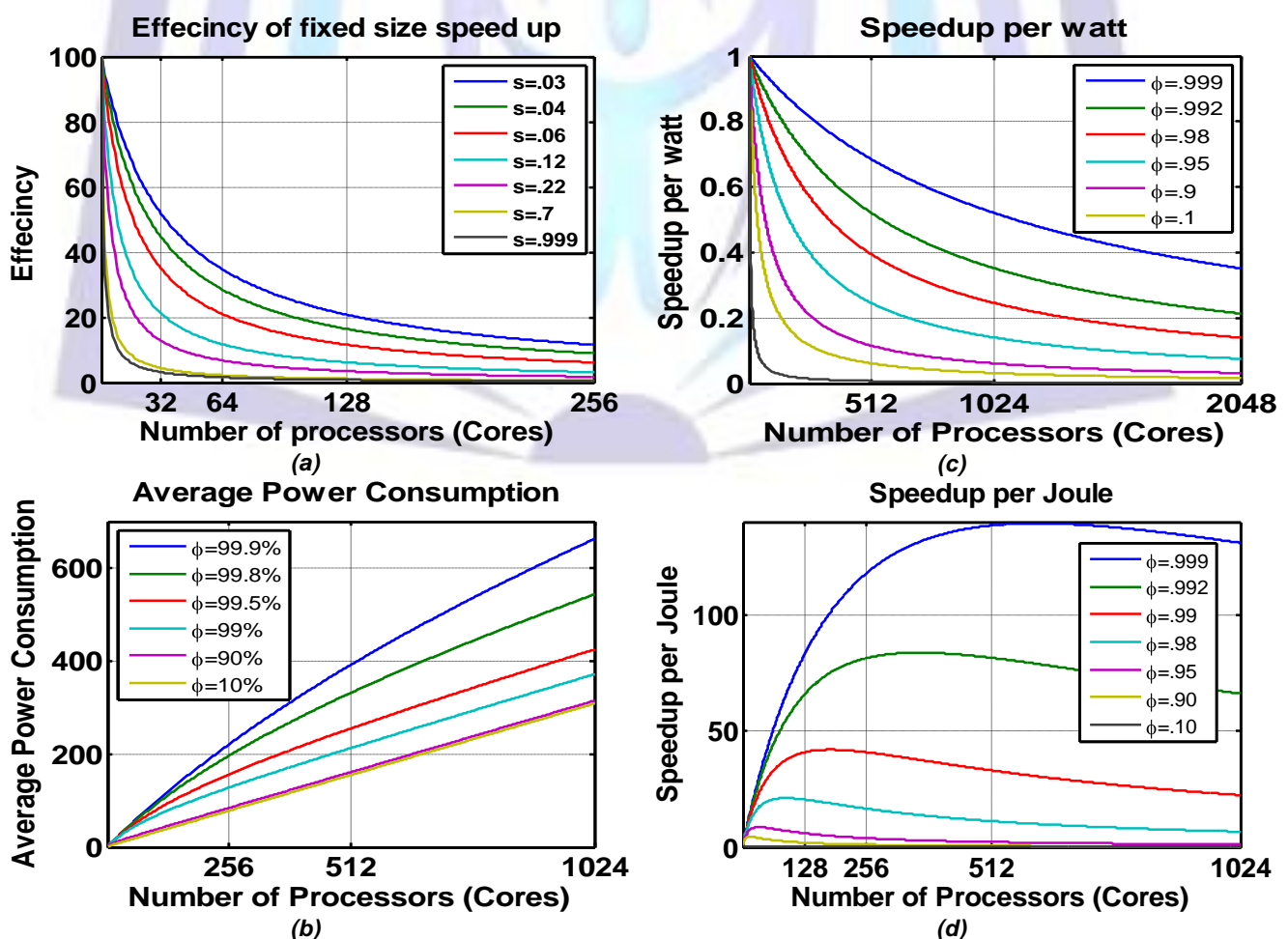




Fig. 4: Fixed-size performance model, (a) Efficiency with impact of serial percentage of code on parallel speedup with number of processors, (b) Average consumption power with the number of processors for different fraction, (c) Speedup per Watt when the number of cores is varied for different fraction of program operations executed sequentially on a single processor and (d) Speedup per joule when the number of cores is varied for different fraction of program operations executed sequentially on a single processor.

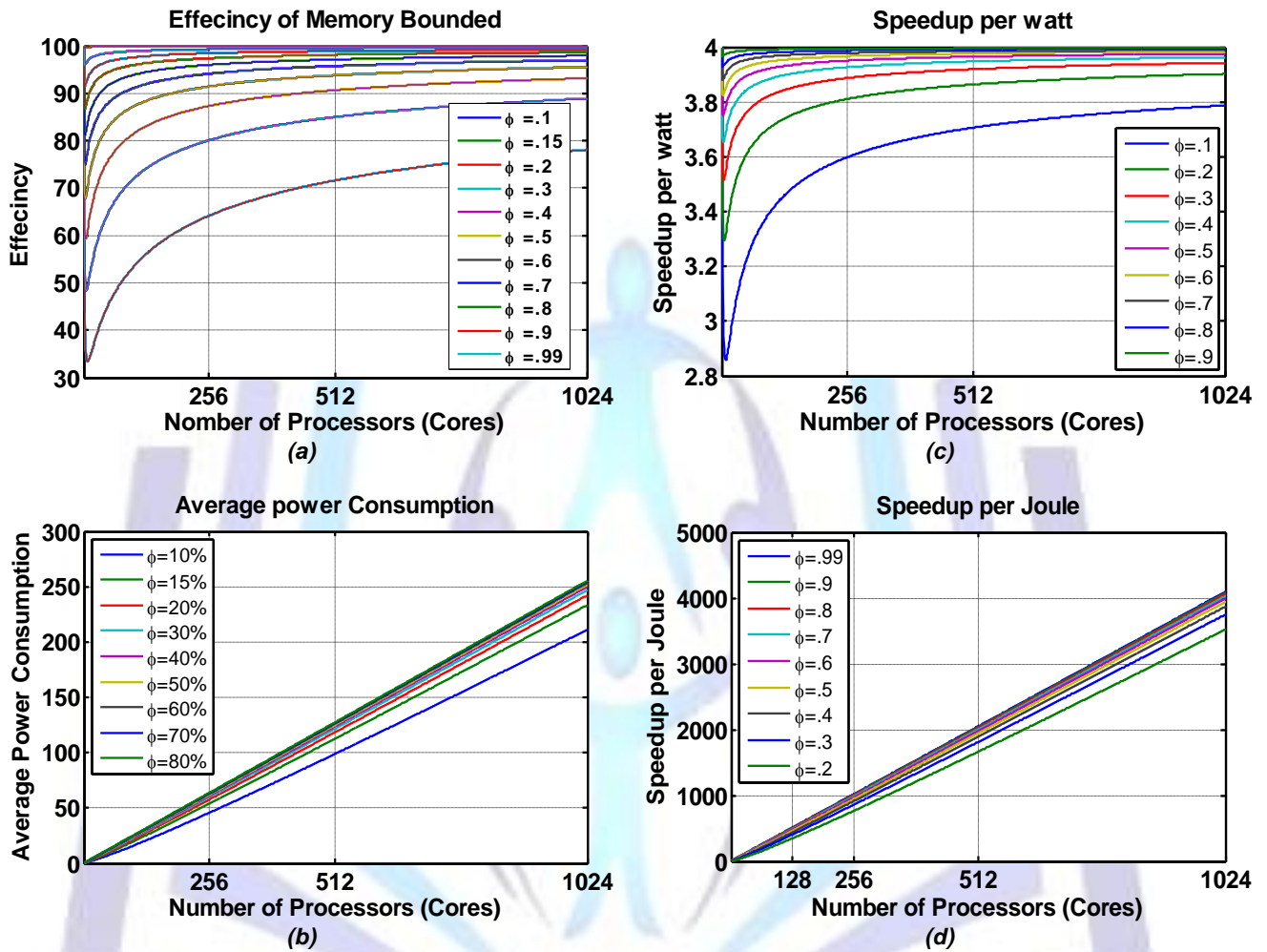




Fig. 5: Memory bounded model, (a) Efficiency of Memory bounded model with number of processors, (b) Average power consumption varying with the number of processors for different fraction of program operations executed sequentially on a single processor, (c) Speedup per Watt when the number of cores is varied from 1 to 1024 for different fraction of program operations executed sequentially on a single processor and (d) Speedup per joule with number of cores for different fraction of program operation executed sequentially on a single processor.

VIII. CONCLUSION

The complete design and implementation of CiComp for AuthGs in their efforts to carry out control and follow up MEEE development project in a systematic manner is investigated. It can be considered as a reference for international cooperation in CiComp development. The approach used in CiComp of MEEE is based on a CiComp approach model considering the organization as a CiComp. The model of CiComp of MEEE is different to earlier models proposed and applied with some success by AuthGs. Parallelization improves the performance of programs for solving large, complex scientific and engineering design problems. Algorithms are used to describe the performance include execution time, speedup, power efficiency, energy and cost as the number of cores increases into account. The aforementioned techniques for enhancement speedup and further reduction the number of processor can be used individually or in combination. The combined technique of performance of the processor and power is presented by demonstrating the design of cloud computing. A simple extension to multi-core cost model to develop an intuition for the impact of the uncore on a many-core processor has been made. Additionally, the analyze multicore of the CiComp scalability, performance and power under fixed-size and memory-bound conditions and from the data access memory wall perspective are studied. These results complement existing studies and demonstrate that CiComp architectures are capable of extensive scalability and developing.

References

- [1] Bengt Ahlgren, Perodro A. Aranda, Prosper Chemouil, Sara Oueslate, Luis M. Correia, Holger Karl, Michael Sollner and Annikki, "Content, Connectivity, and Cloud Ingredient for The Network of Future", IEEE Communications Magazine, Vol. 49, No. 7, pp.(62-70), July 2011.
- [2] Shirlei Aparecida de Chaves, Rafel Brundo Uriarte and Carlos Becker Wastphall, "Toward an Architecture for Monitoring Private Clouds", IEEE Communications Magazine, Vol. 49, No. 12, pp.(130-137), December 2011.
- [3] Amitabh Mishra, Raj Jain Arjan and Arjan Durrest, "Cloud Computing: Networking and Communication Challenges", IEEE Communications Magazine, Vol. 50, No. 9, pp.(24-25), September 2012.
- [4] Luis M. Contreras, Vector Lopez, Oscar Gonzalez de Dios, Alejandro Tovar, Fernando Munoz, Amanda Azanon, Juan Pedro Fernandez-Palacios and Jesus Fogueira, "Toward Cloud-Ready Transport Networks", IEEE Communications Magazine, Vol. 50, No. 9, pp.(48-57), September 2012.
- [5] Chathuranga Widanapathirana Jonathan Li Y. Ahmet Sekercioglu, Milosh Ivanovich and Paul Fitzpatrick, "Intelligent Automated Diagnosis of Client Device Bottlenecks in Private Clouds", 2011 Fourth IEEE International Conference on Utility and Cloud Computing, pp.(261-266), 2011.
- [6] Dan C. Marinescu, "Cloud Computing: Theory and Practice", Computer Science Division Department of Electrical Engineering and Computer Science University of Central Florida, Orlando, FL 32816, USA, Size: 404 Pages, December 6, 2012.
- [7] Jerry Gao, Xiaoying Bai and Wei-Tek Tsai, "Cloud Testing-Issues, Challenges, Needs and Practice", Software Engineering : An International Journal (SEIJ), Vol. 1, No. 1, SEPTEMBER 2011.
- [8] Euisin Lee, Eun-Kyu Lee, Mario Gerla and Soon Y. Oh, "Vehicular Cloud Networking: Architecture and Design Principles", IEEE Communications Magazine, Vol. 52, No. 2, pp.(9-23), February 2014, pp.(148-155).
- [9] Anna Tzanakaki, Markos Anastasopoulos, Konstantinos Geeorgakilas, Giada Landi, Giacomo Bernini, Nicola Ciulli, Jordi Ferrer Riera, Eduard Escalona, Joan A. Garcia-Espin, Xavier Hesselbach, Sergi Figuerola, Shuping Peng, Reza Nejabati, Simeoidou, Damian Parniewicz, Bartosz Belter and Juan Rodriguez Martinez, "Planning of dynamic virtual optical cloud infrastructures: The GEYSERS approach", IEEE Communications Magazine, Vol. 52, No. 1, pp.(26-34), January 2014.
- [10] Roberto Sabella, Francesco Testa, Paola Iolovanna and Giulio Bottari, "Flexible Packet-Optical Integration in Cloud Age: Challenges and Opportunities for Network Delaying", IEEE Communications Magazine, Vol. 52, No. 1, pp.(35-43), January 2014.
- [11] Chen Shan, Chang Heng and Zou Xianjun, "Inter-Cloud Operation via NGSON", IEEE Communications Magazine, Vol. 50, No. 1, pp.(82-89), January 2012.
- [12] Jens Zander and Petri Mahonen, "Riding the Data Tsunami in the Cloud: Myths and Challenges in Future Wireless Access", IEEE Communications Magazine, Vol. 51, No. 3, pp.(145-151), March 2013.



- [13] SivadonChaisiri, Bu-Sung Lee and DusitNiyato, " Optimization of Resource Provisioning Cost in Cloud Computing", IEEE Transactions on Services Computing, Vol. 5, No. 2, pp.(164-177), April-June 2012.
- [14] Gene M. Amdahl, "Validity of the single Processor Approach to Achieving Large Scale Computing Capabilities", AFIPS spring joint computer conference, pp.(1-4), 1967.
- [15] John L. Gustafson, "Reevaluating Amdahl's Law" Communications of the ACM, Volume 31 Number 5, pp.(532-533), May 1988.
- [16] Mark D. Hill and Michael R. Marty, "Amdahl's Law in the Multicore Era", IEEE Published by the IEEE Computer Society, pp.(33-37), July 2008.
- [17] B. Tsilker and S. Orlov, "Computing Efficiency Metrics for Synergic Intelligent Transportation Systems", Transport and Telecommunication, Volume 11, No 4, pp.(66–74), 2010.
- [18] Jee Choi, AparnaChandramowliswaran and Kamesh Madduri, Richard Vuduc, "A CPU–GPU Hybrid Implementation and Model-Driven Scheduling of the Fast Multipole Method", Preprint To appear in GPGPU-7 <http://www.ece.neu.edu/groups/nucar/GPGPU/GPGPU7/>, GPGPU-7, Salt Lake City, UT, USA <http://dx.doi.org/10.1145/2576779.2576787>, March 01 2014.
- [19] StijnEyermanand LievenEeckhout, " Modeling Critical Sections in Amdahl's Law and its Implications for Multicore Design ", ISCA'10, Saint-Malo, France, pp.(1-8), June 19–23, 2010.
- [20] Trevor Mudge University of Michigan "Power: A First-Class Architectural Design Constraint", IEEE Help Shape Future Technologies Computer Society, pp.(52-58), April 2001.

