Design of BPSK Modulator Using VHDL

Mamtha Shetty

PG Scholar

Dept   E & CE

S.D.M. College of Engineering & Technology, Dharwad-02

Email: mamthashetty.46@gmail.com

Phone:+91-9980604132

ABSTRACT

Binary Phase Shift Keying represents the simulation results of binary digital modulation schemes. Here for BASK and BPSK modulation techniques use FPGA algorithm. If multiplier block is used for multiplication bit stream with carrier signal, used time will rises. In addition using multiplier block obtained simulation results were analyzed and compared to other simulation results. Source consumptions of FPGA-based BASK modulation technique and BPSK modulation technique were compared. Also, for different modulation algorithm, source consumptions of BASK and BPSK modulation technique were analyzed using VHDL. Designed modulators using VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) was realized on high speed FPGA (Field Program Programmable Gate Array). Because for used modulation technique data rate transfer is fairly important in wireless communication systems. The highest speed data rate transfer can be realized using fiber optic cables.

In addition, BER (Bit Error Rate) of BASK and BPSK modulator was compared using MATLAB simulation program. Binary data rate is same for BPSK and BASK. BPSK and BASK modulations were designed on FPGA using VHDL hardware description language.

1. INTRODUCTION

Data modulators, especially those intended to produce constant envelope output signals, are "high-leverage" components in that even very small deviations from ideal in their behavior can lead to large degradations in overall system performance. Therefore, successful simulation of wireless communication systems depends upon the use of modulator models that capture all of the significant deviations from ideal behavior.

In the "usual" development of data modulation techniques as presented in most communications texts, the various techniques are presented in order of complexity, starting with the simplest. Thus BPSK would be presented first, then QPSK followed by m-PSK, and so on. Because of its relationship to complex-envelope representations of signals, quadrature modulation plays a central role in simulation of wireless communication systems and models for quadrature modulators, and demodulators serve as building blocks for most other types of data modulators and demodulators.

Despite simple transmitter and receiver architecture of BPSK modulator, BPSK modulation technique is still commonly used in wireless communication such as WPAN (Wireless Personal Area Network) [1]. Amplitude shift keying (ASK) is data transfer technique with different amplitude of carrier frequency. Although it is sensitive to propagation channel variation, ASK modulation has been widely used in low-power wireless transceiver for system simplicity [2].

For low power consumption, wireless communication systems exist in implantable medical devices [3], ingestible capsule endoscopy and multichannel neural recording [4]. The ASK modulation/demodulation scheme, for both RF-band and baseband transceiver, was presented. This design is realized on future mobile memory I/O interface for energy efficient [5]. However, BPSK is as well as showing better Bit Error Rate (BER) compared to BASK. In addition, an analysis was realized about BER achievable in an ASK self-heterodyne optical millimeter-wave system. In this work, it was shown that the need for a depressed decision threshold to optimally detect the received signal [6].

BPSK and BASK modulation techniques were implemented on EP3C40F780C6 FPGA device. Simulation results consist of bit error rate of BASK and BPSK, source consumption of BASK and BPSK.

In addition to, bit error rate of BPSK modulation techniques was compared using MATLAB. Finally, simulation results were compared. BASK and BPSK modulation techniques are binary shift keying. BASK modulation technique based on amplitude while BPSK modulation technique based on phase. According to transmitting data, phase or amplitude is changed.

If "1" was transmitted, the modulated signal remained the same as the carrier, with 0º initial phase, but if "0" was transmitted, the modulated signal would change with 180º, like shown in fig. 1. The aim is to generate BPSK modulation which is a popular modulation technique used in communication industry, thus its symbol error performance and bandwidth efficiency. If "1" was transmitted, the modulated signal remained the same as the carrier, with 0º initial phase, but if "0" was transmitted, the modulated signal would change with 180º, like shown in fig. 1.The aim of the paper is to generate BPSK modulation which is a popular modulation technique used in communication industry, thus its symbol error performance and bandwidth efficiency.

2. BPSK Modulation

In BPSK, individual data bits are used to control the phase of the carrier. During each bit interval, the modulator shifts the carrier to one of two possible phases, which are 180 degrees or π radians apart. This can be accomplished very simply by using a bipolar baseband signal to modulate the carrier's amplitude, as shown in fig. The output of such a modulator can be represented mathematically as

$$x(t) = R(t) \cos(\omega ct + \theta)$$

For BPSK modulation technique based on phase modulation, BPSK modulation is realized with changed phase. For example, in fig 2, beginning of BPSK modulated signal's period is positive values, if transmitting symbol is 1. But if transmitting signal is 0, beginning of BPSK modulated signal's period is negative values. BPSK modulated signal is change at this cases. In fig 1, it is shown that principle of BPSK modulator. Binary data is converted to binary code bipolar format, then binary code bipolar format signal is multiplied carrier signal.
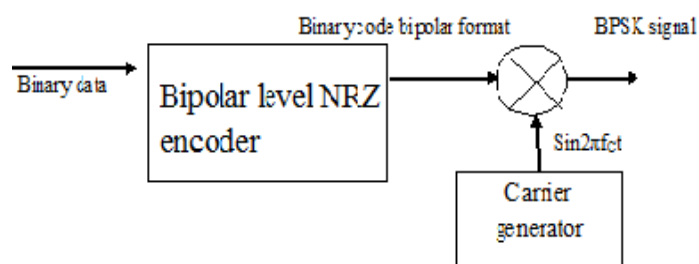
Fig1: Principle of BPSK modulator

Thereby, BPSK modulated signal is created. In Fig 2, it is shown that BPSK modulation. In this fig, m(t) is waveform of bipolar format, c(t) is carrier signal and s(t) is modulated signal.
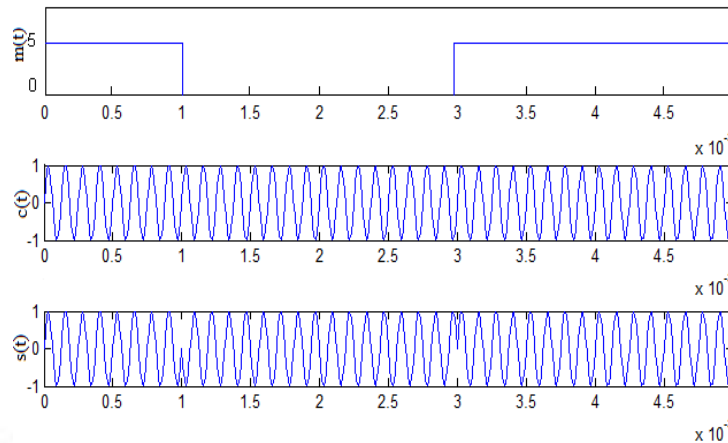

Fig 2. BPSK Modulation

In BPSK, the transmitted signal is S(t)=m(t)c(t) & f_c is the frequency of the carrier, BPSK demodulator can be achieved from the BPSK waveform by using scheme of modulator in fig 3. The most important point for receiver, received signal is obtained quite correctly. As realizing in modulator input signal is firstly multiplied with a carrier of signal in demodulator. Next, multiplied signal is passed through integrator, then integrated signal is passed through a decision making device.
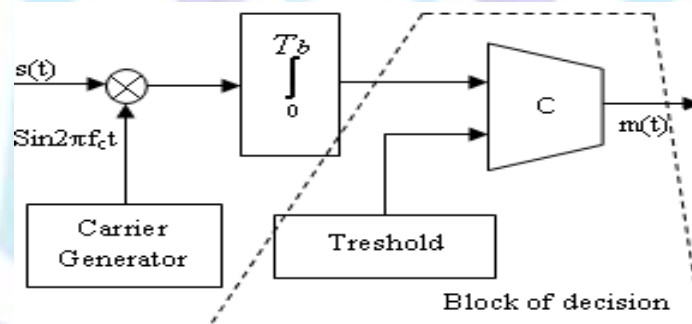

Fig 3. Principle of BPSK and BASK Modulator.

A BPSK modulator which is constituted by a random data generator, the BPSK modulator itself and a DAC interface device . As we can see in the figure, the data generator has two inputs (clk and reset) and two outputs (data and sync), whereas the BPSK modulator has three inputs (clk, reset and serial data) and three outputs (clk_data, clk_spi and data). Moreover, the output clk_data is fed back to the clock input of the data generator, whereas the output of the latter is connected to the serial data input of the BPSK modulator
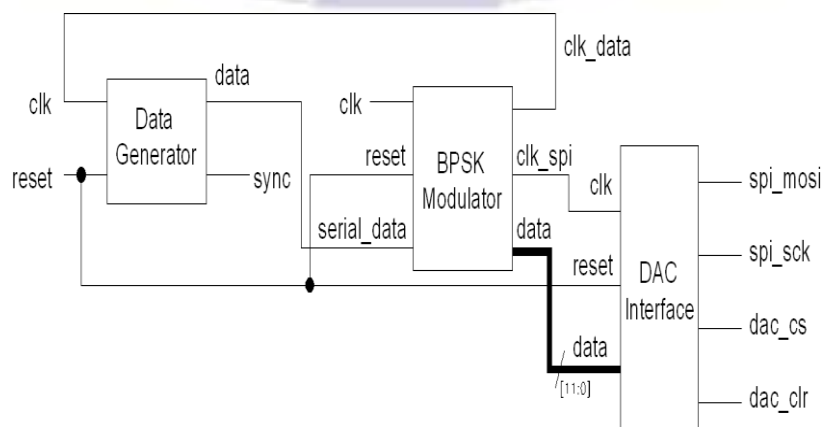

Fig 4. Block diagram of the BPSK system

Given that the output of the BPSK modulator has to be analog, a DAC interface is included to establish the communication with this device by means of the SPI bus. The BPSK modulator supplies the clock reference signal for the SPI bus, as well as the digital data word which must be converted to analog by the DAC. Therefore, the BPSK modulator is in charge of controlling the synchronism of all the system components, generating the clock signals for the SPI bus, as well as those for the data generator and the modulator itself

2.1 DAC Interface

The device which works as DAC interface has three inputs (reset, clk and data) and four outputs corresponding to the communication wires of the SPI bus (spi_mosi, spi_sck, dac_cs, dac_clr). Next we are going to design this interface with the DAC, which will allow us to represent an analog signal through channel DAC A.

As the controller of the DAC interface is basically constituted by a state machine based on the variable count. Every time that there is a rising edge of the signal clk, this variable is increased and several conditions are checked. If count is equal to one, the data are loaded to the memory of the interface (memory_dac) and the latter is prepared for the transmission of the data towards channel DAC A through the SPI bus. Once the 32 data bits are transmitted, the signal dac_cs is set to high logic level in order to indicate to the DAC that initiates the conversion, re-initiating all the process again. This process is repeated endlessly, unless this is interrupted by a reset signal, which would initialize the interface. We can see as the spi_sck and dac_clr signals are obtained by simply inverting the clk and reset signals, respectively.

Now, we are going to carry out a simulation by using the ISE Simulator in order to check the correct behaviour of the interface with the DAC. Observe as a signal of type std_logic_vector called count_out has been included with the unique mission of making easier the analysis of the different signals of the device.

2.2 Data generator

For the design of the pseudo-random data generator we can use that implemented in the previous practice. This data generator requires from the definition of several constants and a component which works as register.

Apart from the constant N which is referred to the length (number of registers) of the data generator and the and_vector function which determines the and-logic function of a data vector, are also defined a constant M for the number of positions of a table which is going to contain the sine wave values, the number of bits (nbits) of each word of the table, as well as the number of bits used as decimals (ndec), and two real constants (Pi and delta_phi). The two last ones are used by a function which initializes the table and they are referred to the irrational number π and the phase increment ϒ ψ between consecutive positions in the table which is given by 2π/M.

Modulator

First of all, we have to take into account that, considering the way in which the DAC interface has been defined, this device requires from 64 clock cycles in order to carry out the transmission of the digital data to be represented by the DAC in an analog way. Therefore, the clock to be used by this device will be the fastest one, that is, the on-board 50 MHz clock oscillator. During these 64 clock cycles, the data supplied by the DAC is not allowed to change, therefore the modulator clock which controls the addressing to the sine wave table has to oscillate at a frequency 64 times slower than that of the basis clock. Moreover, the data supplied by the generator, which modulates the sine wave, must be maintained unalterable during at least a complete cycle of the sine wave, which is constituted by M samples, hence the data clock has to oscillate at a frequency M times slower than that of the table addressing. Taking into account everything that has previously been mentioned, it is possible to define the rhythm of the different clock signals generated by the BPSK modulator, but it is also necessary to create the table which contains the values of the different samples of the sine wave. Thus, we are going to create a package, which we are going to name real2bit, where all the functions necessary to generate the table are defined.

3. Applications of BPSK Modulator

Owing to PSK's simplicity, particularly when compared with its competitor quadrature amplitude modulation, it is widely used in existing technologies.

The wireless LAN standard, IEEE 802.11b-1999,[1][2] uses a variety of different PSKs depending on the data-rate required. At the basic-rate of 1 Mbit/s, it uses DBPSK (differential BPSK). To provide the extended-rate of 2 Mbit/s, DQPSK is used. In reaching 5.5 Mbit/s and the full-rate of 11 Mbit/s, QPSK is employed, but has to be coupled with complementary code keying. The higher-speed wireless LAN standard, IEEE 802.11g-2003[1][3] has eight data rates: 6, 9, 12, 18, 24, 36, 48 and 54 Mbit/s. The 6 and 9 Mbit/s modes use OFDM modulation where each sub-carrier is BPSK modulated. The 12 and 18 Mbit/s modes use OFDM with QPSK. The fastest four modes use OFDM with forms of quadrature amplitude modulation.

Because of its simplicity BPSK is appropriate for low-cost passive transmitters, and is used in RFID standards such as ISO/IEC 14443 which has been adopted for biometric passports, credit cards such as American Express's ExpressPay, and many other applications.[4]

Bluetooth 2 will use $\pi/4$-DQPSK at its lower rate (2 Mbit/s) and 8-DPSK at its higher rate (3 Mbit/s) when the link between the two devices is sufficiently robust. Bluetooth 1 modulates withGaussian minimum-shift keying, a binary scheme, so either modulation choice in version 2 will yield a higher data-rate. A similar technology, IEEE 802.15.4 (the wireless standard used by ZigBee) also relies on PSK. IEEE 802.15.4 allows the use of two frequency bands: 868–915 MHz using BPSK and at 2.4 GHz using OQPSK.

Notably absent from these various schemes is 8-PSK. This is because its error-rate performance is close to that of 16-QAM — it is only about 0.5 dB better but its data rate is only three-quarters that of 16-QAM. Thus 8-PSK is often omitted from standards and, as seen above, schemes tend to 'jump' from QPSK to 16-QAM (8-QAM is possible but difficult to implement).

Included among the exceptions is HughesNet satellite ISP. For example, the model HN7000S modem (on KU-band satcom) uses 8-PSK modulation.

BPSK (also sometimes called PRK, phase reversal keying, or 2PSK) is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180° and so can also be termed 2-PSK. It does not particularly matter exactly where the constellation points are positioned, and in this figure they are shown on the real axis, at 0° and 180°. This modulation is the most robust of all the PSKs since it takes the highest level of noise or distortion to make the demodulator reach an incorrect decision. It is, however, only able to modulate at 1 bit/symbol (as seen in the figure) and so is unsuitable for high data-rate applications.

In the presence of an arbitrary phase-shift introduced by the communications channel, the demodulator is unable to tell which constellation point is which. As a result, the data is often differentially encoded prior to modulation. BPSK is functionally equivalent to 2-QAM modulation.

The general form for BPSK follows the equation:

$$s_n(t) = \sqrt{\frac{2E_b}{T_b}} \cos(2\pi f_c t + \pi(1 - n)), n = 0, 1.$$

This yields two phases, 0 and π. In the specific form, binary data is often conveyed with the following signals:

$$s_0(t) = \sqrt{\frac{2E_b}{T_b}} \cos(2\pi f_c t + \pi) = -\sqrt{\frac{2E_b}{T_b}} \cos(2\pi f_c t)$$ for binary "0"

$$s_1(t) = \sqrt{\frac{2E_b}{T_b}} \cos(2\pi f_c t)$$ for binary "1"

where f_c is the frequency of the carrier-wave.

Hence, the signal-space can be represented by the single basis function

$$\phi(t) = \sqrt{\frac{2}{T_b}} \cos(2\pi f_c t)$$

where 1 is represented by $\sqrt{E_b}\phi(t)$ and 0 is represented by $-\sqrt{E_b}\phi(t)$. This assignment is, of course, arbitrary.
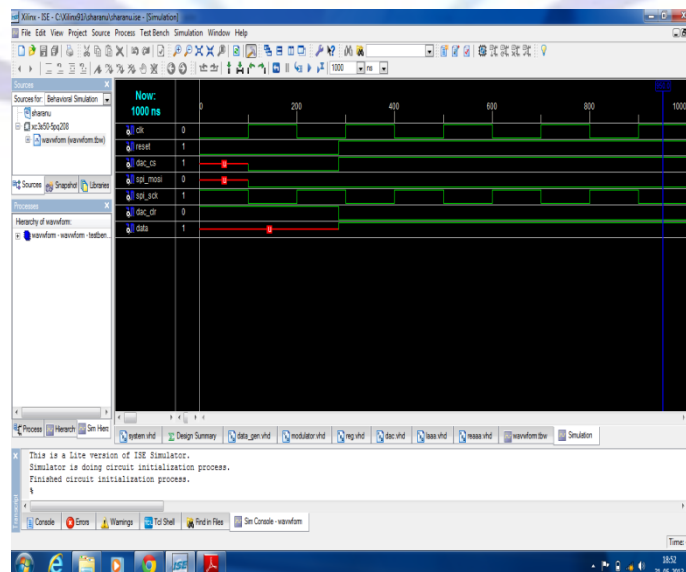
4. Simulation Result:

Fig 5. Simulation Results

In fig, it is shown that simulation result of the BPSK modulation. In d_in represent input of bit_separator and digital output of ADC. So Floating Point numbers is multiplied, BPSK signal (output of modulator) has hexadecimal format. This hexadecimal format is represented 32 bits. This numbers can be converted to decimal form using MATLAB. Because hexadecimal numbers are samples of BPSK signal, this numbers are converted to decimal form then plotting of BPSK signal can be created using plotting program. Figure in plotting program (BPSK modulated signal) is obtained. According to bit value of d_out (output of bit_separator), output of mux (phase of BPSK signal) are selected. Counter is number of transmitted samples. During transmit to one symbol, 500 samples are transmitted. Thanks to used control block, one symbol is transmitted bit per 500 samples.

5. Conclusion:

BPSK and BASK modulation techniques based on FPGA. Also, comparison to performance of implemented modulation techniques are analyzed It is shown that modulation techniques (BASK and BPSK) have disadvantage and advantage in simulation and plotting results. In this results, it is illustrated that BER of BASK high than BER of BPSK. Yet, bit transfer rate of BASK is as same as bit transfer rate of BPSK. Also, power consumption of BASK is low than BPSK. As shown source consumption for BASK modulation is less than BPSK modulation. It is shown that used ROM numbers less than it. But used multiplier is more than it. In addition to, it is shown that changing of bit (0-1-0) is realized on each 500 sample. In BASK modulator, for 0 bit, it is shown that sending data is 0 while for 1 bit, it is shown that sending data is samples of carrier signal. In BPSK modulator, for 0 bit, it is illustrated that processing data is samples of delayed carrier signal (180 degrees of phase delay), for 1 symbol, it is illustrated that processing data is samples of carrier signal.

After implementing the BPSK modulator, we want to realize a BPSK system. The system will consist of a modulator and demodulator and the signal from the modulator to demodulator will pass through a channel affected by AWGN (Additive White Gaussian Noise). The modulated and demodulated signals will be also routed to VGA monitors, but also to oscilloscopes.

6. References:

[1] Park, H., C., "Power and bandwidth efficient constant-envelope BPSK signals and its continuous phase modulation", IEE Proceedings Communications, vol. 152, No. 3, June 2005

[2] Jae, C., M., Eon, J., S., "Design of Low Power ASK CMOS Demodulator Circuit for RFID Tag", 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), pp. 1-4, 2010.

[3] Sanni, A., Vilches, A., Toumazou, C.," Inductive and Ultrasonic Multi-Tier Interface for Low-Power, Deeply Implantable Medical Devices", Transactions on Biomedical Circuits and Systems, vol. PP, pp. 1-12, 2012

[4] Diao, S., Zheng, Y., Gao, Y., Cheng, S., J., Yuan, X., Je, M., Heng, C.," A 50-Mb/s CMOS QPSK/O-QPSK Transmitter Employing Injection Locking for Direct Modulation", Microwave Theory and Techniques, IEEE Transactions on, vol. 60, pp. 120-130, 2012.

[5] Byun, G.,S., Kim, Y., Kim, J., Tam, W.-S., Chang, F., "An Energy-Efficient and High-Speed Mobile Memory I/O Interface Using Simultaneous Bi-Directional Dual (Base+RF)-Band Signaling", IEEE Journal Of Solid-State Circuits, Vol. 47, No. 1, January 2012

[6] Lane, P., M., Kitayama, K., "The interaction between fibre dispersion and laser phase noise in an ASK self-heterodyne millimetre-wave fibre-radio system", IEE Proceedings Optoelectronics, vol. 146, no. 4, August 1999.

[7] Das, A., "Digital Communication: Principles and System Modelling ", Springer-Verlag Berlin Heidelberg, 2010.