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Design and Performance Investigation of a New Distributed Amplifier Architecture for 40 and 100 Gb/s Optical Receivers

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ABSTRACT

The design of distributed amplifiers (DAs) is one of the challenging aspects in emerging ultra high bit rate optical communication systems. This is especially important when implementation in submicron silicon complementary metal oxide semiconductor (CMOS) process is considered. This work presents a novel design scheme for DAs suitable for front-end amplification in 40 and 100 Gb/s optical receivers. The goal is to achieve high flat gain and low noise figure (NF) over the ultra wideband operating bandwidth (BW). The design scheme combines shifted second tire (SST) matrix configuration with cascode amplification cell configuration and uses m-derived technique. Performance investigation of the proposed DA architecture is carried out and the results are compared with that of other DA architectures reported in the literature. The investigation covers the gain and NF spectra when the DAs are implemented in 180, 130, 90, 65 and 45 CMOS standards.The simulation results reveal that the proposed DA architecture offers the highest gain with highest degree of flatness and low NF when compared with other DA configurations. Gain-BW products of 42772 and 21137 GHz are achieved when the amplifier is designed for 40 and 100 Gb/s operation, respectively, using 45 nm CMOS standard. The simulation is performed using AWR Microwave Office (version 10).

Indexing terms/Keywords

Distributed Amplifier; 40Gb/s Distributed amplifier; 100Gb/s Distributed amplifier

Academic Discipline And Sub-Disciplines

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1- INTRODUCTION

Everybody wants to benefit from the evaluation in the field of communication especially through internet. Due to the expanding demand of communication services, the volume of data exchanged in the communication systems has increased. This leads to increase data rate of the global communication systems from tens of Gb/s to Tb/s. BW requirements will increase by more than 100 times and applications such as virtual reality require data rate that are 10,000 times higher than currently available. To transport such data rate, a media with low loss and high BW is required [1, 2]. Among the available medium to transfer the data, optical fibers have the best performance. Optical fibers are very common these days to transport very high rate digital data. Such high speed data rates can be transported over kilometers of optical fiber and without significant loss. Normally loss is very low when the signal is transmitted using light rather than electrical signal. These fibers also have the advantage of being low cost in addition to improvement of performance. Fiber optic devices and systems are evidently employed to realize very high data rates. Fiber optic communication is a solution because high data rates can be transmitted through this high capacity cable with high performance [3].

The exponential growth of Internet traffic is fueling the research and development of wavelength division multiplexed passive optical network technology in the access network segment [4]. Driven by the continues increase in BW demand and number of subscribers, future access networks will require 40 Gb/s high speed service per wavelength channel [5, 6] on a 50 GHz dense wavelength grid. The realization of high-speed analog-to-digital conversation and digital signal processing have enabled a bit rate of 100 Gb/s in long-haul coherent optical communication system [7]. However, for short-reach 100 Gb/s applications, solutions that use intensity modulation and direction detection are seen as more practical [8]. With the advances in semiconductor technologies, integrated circuits operating at 40 Gb/s have been realized in standard CMOS process [9]. Among all kinds of high speed circuits, the broadband amplifier is a key building block at both the transmitting and receiving ends, see Fig. 1. In fact there is demand for wideband CMOS amplifiers in the front-end section of the optical receivers. Distributed amplification is one of the well-known methods to provide such performance by absorbing the parasitic capacitances of parallel gain distributed cell into an artificial transmission line, which in return, guarantees the gain uniformity and input/output matching within the BW of operation. However, design DA for 40 Gb/s (and above) optical receivers needs careful consideration related to the gain, frequency spectrum and NF.This paper addresses the design issues and performance investigation of CMOS DA for the front-end amplification stage in 40 and 100 Gb/s optical receivers.

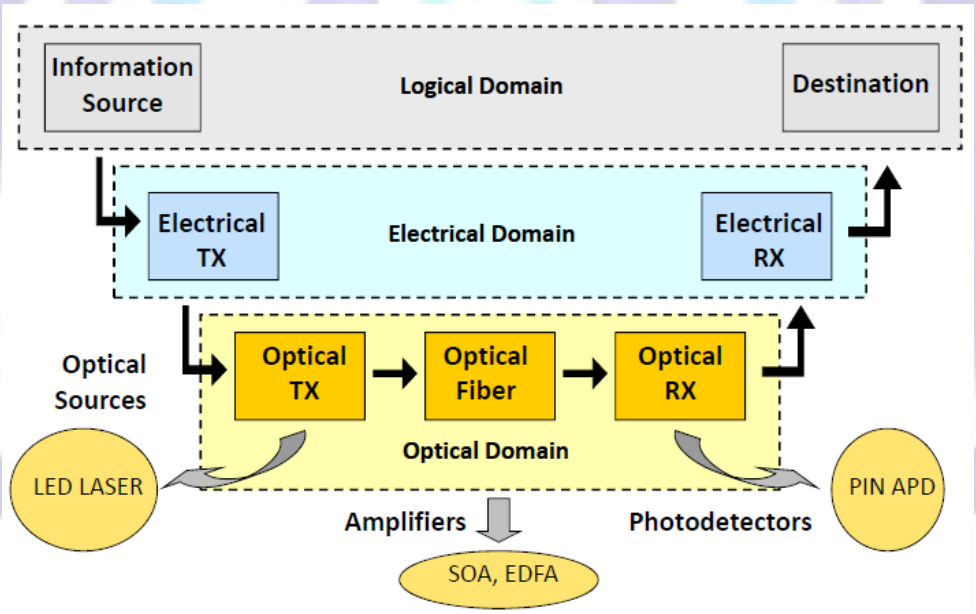

Figure 1: Optical communication system [10].

2- RELATED WORK

In 2005, Wolf et al [11] demonstrated an eight-stage DA with 12.5 dB ± 0.45 dB gain and 50 GHz BW in a commercially available 0.1 μm metamorphic GaAs HEMT technology. The amplifier has a minimum NF lower than 2.5 dB in the BW. The group delay variation from 9 to 40 GHz is ± 7.5 ps and circuit power consumption is 0.4 W. Such amplifier packaged with a high responsively PD into a fiber pig-tailed module. Eye diagrams measurements demonstrate the successful high-speed operation of the photoreceiver.

In 2007, Chien and Lu [12] presented a novel circuit topology for high-gain 40 Gb/s DAs. Based on the conventional distributed architecture, the gain cells were realized by cascading cascode stages for gain enhancement. In addition, the stagger-tuning technique was extensively utilized in the design of the cascode stages as well as the cascaded stages, leading to significant improvement in terms of the operating BW and the gain flatness. With the proposed circuit architecture, two amplifiers were implemented in a standard 180 nm CMOS technology. The amplifier with a 3 x3 configuration exhibits a gain of 16.2 dB and a 3 dB BW of 33.4 GHz, while the one in a form of 2x4 demonstrates a gain of

20 dB and a BW of 39.4 GHz. Consuming a DC power of 260 mW from a 2.8-V supply voltage, both circuits provide clear eye-opening with a pseudorandom bit sequence at 40 Gb/s.

In 2009, Moez and Elmasry [13] presented a circuit technique to compensate for the metal and substrate loss of the on-chip transmission lines, and, consequently, to improve the gain flatness and BW of CMOS DAs for optical receivers. An eight-stage DA suitable for 40 Gb/s optical communication was devised and implemented in a 130 nm CMOS process. The DA achieves a flat gain of 10 dB from DC to 44 GHz with an input and output matching better than −8 dB. The measured NF varies from 2.5 to 7.5 dB with the amplifier's band. The proposed DA dissipates 103mW from two 1-V and 1.2-V DC supplies.

In 2009, Entesari et al [14] presented a state-of-the-art DA with coupled inductors in the gate line. The proposed coupled inductors, in conjunction with series-peaking inductors in cascode gain stages, provide BW extension with flat gain response for the amplifier without any additional power consumption. On the other hand, gate-inductor coupling improves the input matching of the amplifier considerably. The detailed analysis and design methodology for the proposed DA were presented. The new four-stage DA, fabricated using an IBM 0.18- m CMOS process, achieves a power gain of around 10 dB, input and output return losses better than 16 and 18 dB, respectively, a NF of 3.6–4.9 dB, and a power consumption of 21mW over a 16-GHz flat 1-dB BW. is between 0.1 and 3.75 dBm across the entire band.

In 2010, Ghadiri and Moez [15] presented a new high-gain structure for DA. Negative capacitance cells were exploited to ameliorate the loading effects of parasitic capacitors of gain cells in order to improve the gain of the DA while keeping the desired BW. In addition, the negative capacitance circuit creates a negative resistance that can be used to increase the amplifier BW. Implemented in 130 nm IBM's CMRF8SF CMOS, the proposed six-stage DA presents an average gain of 13.2 dB over a BW of 29.4 GHz. The measured input return loss is less than 9 dB and the output return loss is less than 9.5 dB over the entire BW. With a chip area of 1.5 mm X 0.8 mm, the amplifier consumes 136 mW from a 1.5-V DC power supply.

In 2010, Chien et al [16] presented a transimpedance amplifier (TIA) with a tunable BW for optical communications. The proposed TIA is composed of two cascaded stages in which an input network with inductive peaking elements is employed in the first stage for broadband operations while a modified DA is utilized as the second stage for enhanced transimpedance gain. In addition, a feedback loop is incorporated as the bandwidth-tuning mechanism. By tuning the BW of the TIA, optimum circuit operation with lowest bit error rate (BER) can be achieved in the receiver front end for high-speed data transmission. The proposed circuit was implemented in a 180 nm CMOS process. Consuming a DC power of 33.3 mW from a 1.8-V supply, the fabricated TIA exhibits a transimpedance gain of 47.8 dB and a variable 3-dB BW from 6.2 to 10.5 GHz. Providing a 2^{11}-1 pseudorandombit sequence at 9-15 Gb/s, a BER less than 10^{-12} was demonstrated experimentally by the TIA with the BW tuning mechanism.

In 2011, KimandBuckwalter [17] demonstrated a low-power cascode DA in a 45 nm silicon-on-insulator (SOI) CMOS process. The amplifier achieves a 3 dB BW of 92 GHz. The peak gain is 9 dB with a gain-ripple of less 1.5 dB over the BW. The group-delay variation is under ± 4.7ps over the 3 dB BW. The amplifier consumes 73.5mW from a 1.2V supply and results in a GBW efficiency figure of merit of 3.53 GHz/mW. The chip occupies an area of 0.45 mm^2 including the pads.

In 2012, Jahanian and Heydari [18] presented a CMOS DA with distributed active input balun that achieves a GBW product of 818 GHz, while improving linearity. Each cell within the DA employs dual-output two-stage topology that improves gain and linearity without adversely affecting BW and power. Comprehensive analysis and simulations were carried out to investigate gain, BW, linearity, noise, and stability of the proposed cell, and compare them with conventional cells. Fabricated in a 65-nm low-power CMOS process, the 0.9-mm DA achieves 22 dB of gain and a P1dB of 10 dBm, while consuming DC power of 97 mW from a 1.3-V supply. A distributed balun, designed and fabricated in the same process, using the same topology achieves a BW larger than 70 GHz and a gain of 4 dB with 19.5-mW power consumption from 1.3-V supply.

In 2013, Feng et al [19] realized compact self-biased wideband low noise amplifier (LNA) in Global Foundries 65 nm CMOS technology. Wideband input matching characteristic is achieved by placing a series gate inductor and a parallel tuning capacitor in the resistive-feedback network. Combined with the inductive-series peaking technique which further extends the BW, the proposed cascaded three-stage resistive-feedback amplifier obtains a large operating BW which is comparable with the DA. Measurement shows that the proposed amplifier achieves a power gain of with input and output return losses better than 8 dB and NF ranging from 4.5 to 6.8 dB between 2.1–39 GHz. The fabricated low LNA occupies a silicon area of 0.16 including all testing pads and draws 17 mA from a 1.5 V power supply.

In 2013, Kao et al. [20] proposed a new DA topology which is a combination of the conventional DA and the cascaded single-stage DA. This DA topology can provide wide BW with considerations of the gain, NF, and output power simultaneously, and requires reasonable DC power consumption. Two termination methods of this combination were investigated. From the measurements, the first DA has a small-signal gain of 20.5 dB, a 3-dB BW of 35 GHz, and a GBW product of 371 GHz. The maximum output power at 1-dB output compression point is 8.6 dBm and the NF is between 6.8–8 dB at frequencies lower than 18 GHz. The chip size, including testing pads, is only 0.78 mm, and the ratio of the GBW to chip size is 476GHz/mm. The second DA has a small-signal gain of 24dB, a 3-dB BW of 33 GHz, and a GBW product of 523 GHz. The maximum output power is 9 dBm and the NF is between 6.5-7.5 dB at frequencies lower than 18 GHz. The chip size including testing pads is only 0.83 mm, and the ratio of the GBW to chip size is 630 GHz mm.

In 2013, Cho et al. [21] proposed a wideband switchless bi-directional DA in a commercial 130 nm CMOS technology, which realizes multi-octave BW with high gain and low NF using DA technique and cascode amplifier pair. The measured gain is over 10 dB and measured NF is 3.2-6.5 dB. The input and output return losses are better than 9 dB at 3–20 GHz. The measured output power 1dB and output input power (OIP3) is larger than 8 dBm and 17 dBm at 4–15 GHz. The chip sizeis 0.96 x 0.85 mm^2including pads. The proposed switchless bi-directional amplifier has almost the same chip size compared to the conventional uni-directional DA.

In 2014, Kim and Nguyen [22] presented a new tri-band power amplifier on a 180 nm SiGeBiCMOS process, operating concurrently in Ku/K/Ka and -band, is presented. The concurrent tri-band PA design is based on the DA structure with capacitive coupling to enable large device size, while maintaining wide BW, gain cells with the enhanced-gain peaking inductor, and negative-resistance active notch filters for improved tri-band gain response. The concurrent tri-band PA exhibits measured small-signal gain around 15.4, 14.7 and 12.3 dB in the low band (10–19 GHz), midband (23–29 GHz), and high band (33–40 GHz), respectively.

It is clear from the above survey that the reported designs of DAs suitable for high bit rate optical receiver don't achieves simultaneously wide BW, high flat gain and low NF. This issue is addressed in this thesis where a modified DA topology is introduced to reach these goals.

3- PROPOSED DA ARCITECTURE AND DESIGN CONCEPTS

In the literature, different DA architectures have been discussed. Each one has its own design topology and uses different techniques to enhance one of the design requirements: wide BW, high flat gain and low NF. In this section, a new DA architecture is proposed to achieve ultrawide band operation under high amplification gain and low NF conditions. The proposed architecture collects the main features behind different topologies and techniques adopted in previous DA designs such as shifted second stage (SST) topology, matrix configuration, cascode cell amplifier configuration, and m-derived matching technique. Design issues based on deep submicron CMOS technology are discussed toward achieving efficient front-end amplification in 40 Gb/s and 100 Gb/s optical receivers.

3.1 - Architecture of the Proposed Distributed Amplifier

The main idea behind the proposed DA is to combine high-feature topologies and techniques adopted by other DA designs. The task in this work is primarily to design CMOS-based DA with ultrawide BW, high flat gain and low NF suitable for high bit rate optical receivers ($\geq$ 40 Gb/s). The proposed DA uses the following techniques and topologies

a- m-derived technique

m-derived techniques is used at the input and output of constant-k filter sections in order to obtain flat BW and constant impedance matching.

b- Shifted-Second Tire Matrix Configuration

This type of DA uses additive and multiplicative technique to achieve high flat gain. The configuration uses M stages and N distributed cells (N tires). Simulation results show that design the DA with two stages and four distributed cells is sufficient to get the require design target. Using M>2 and N>4 will increase the complexity of the design without offering reasonable performance improvement.

c- Cascode Amplification Cell Configuration

Cascode DA is obtained by adding common-gate amplifier section to the drain line of common-source amplifier stage. Using cascode amplification cells in DA configuration will decrease the variation of the capacitance seen by the transmission line and offer a nearly flat gain over wider BW as compared with the simple common-source amplifier.

The cascode amplifier can be considered as a two-stage amplifier composed of a transconductance amplifier followed by a current buffer [23]. Compared to a single amplifier stage, this combination may have one or more of the following characteristics: higher input-output isolation, higher input impedance, higher output impedance, higher gain or higher BW. Thus cascade configuration can be designed to improve input-output isolation (or reverse transmission) as there is no direct coupling from the output to the input.

Fig. 2a shows a MOSFET cascode amplifier. If one make a small-signal analysis for this amplifier using the simplified small-signal equivalent circuit shown in Fig. 2b, the following results are obtained [23]. The voltage gain

$$Av = \frac{V_{out}}{V_{in}} = -\left(g_{m1}r_{o1} + 1\right) g_{m2}r_{o2} \qquad (1.a)$$

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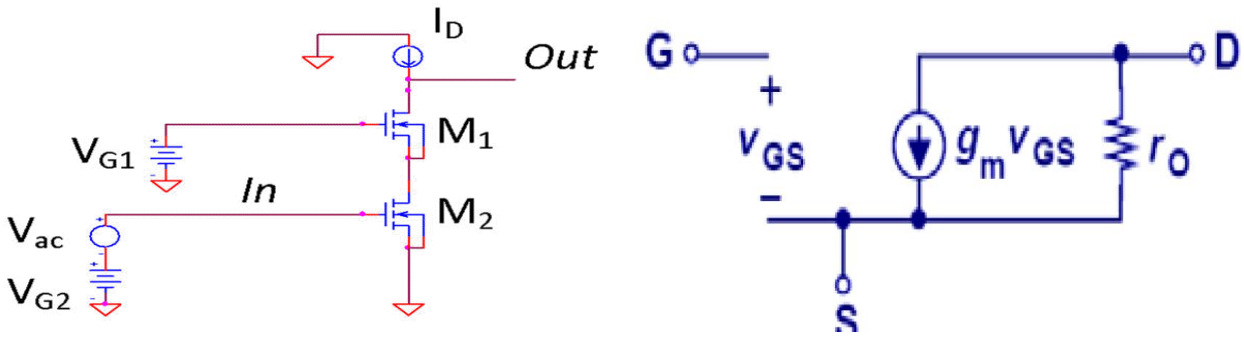


(a) (b)

Figure 2: a- Cascode MOSFET amplifier b- Simplified small-signal equivalent circuit of MOSFET [23].

$$Av \approx g_{m1} g_{m2} r_{o1}\, r_{o2} \quad \text{when } g_{m1} r_{o1} >> 1 \tag{1.b}$$

Note that the cascode amplifier behaves as a common-source amplifier with higher gain. If identical transistor is used, the $Av \approx g_m^2\, r_o^2$. The input resistance of the cascode amplifier tends to infinitely since the input signal source is applied to the high impedance gate terminal.

The output resistance of the cascode amplifier is given by

$$R_{out} = (r_{o1} + r_{o2})(1 + g_{m1}\,(r_{o1} // r_{o2})) \tag{2.a}$$

For identical transistors

$$R_{out} = 2r_o\left(1 + g_m \frac{r_o}{2}\right) \tag{2.b}$$

$$\approx g_m^2\, r_o^2 \quad \text{when } g_m r_o >> 2.$$

This yields higher output impedance compared with conventional common-source amplifier.

Fig. 3 shows a block diagram for the proposed DA configuration. The structure contains two amplification stages each with four amplification cells. The corresponding circuit-level description of the proposed DA is illustrated in Fig. 4.

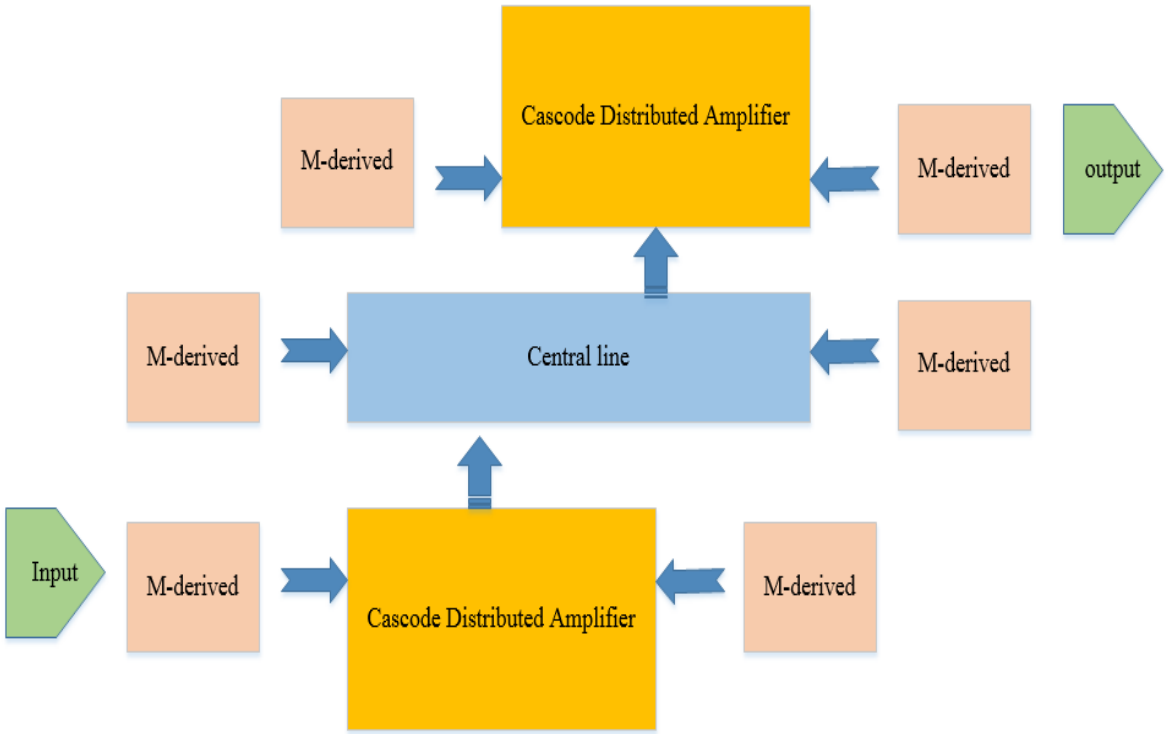


Figure 3: Block diagram of the proposed shifted second tier with m-derived DA.

3.2- Design Concepts

The gate and drain transmission lines are designed with equal inductance and capacitance to ensure equal wave propagation velocities along both lines. The cutoff frequency f_c and characteristic impedance Z_0 of the transmission lines are given by

$$f_c = \frac{1}{\pi\sqrt{L_g C_g}} = \frac{1}{\pi\sqrt{L_d C_d}} = \frac{1}{\pi\sqrt{L_l C_c}} \quad (3.a)$$

$$Z_o = \sqrt{\frac{L_g}{C_g}} = \sqrt{\frac{L_d}{C_d}} = \sqrt{\frac{L_c}{C_c}} \quad (3.b)$$

where L and C stand, respectively, to the inductance and capacitance of the transmission line, while the subscripts g and d denote gate and drain, respectively. For given values of f_c and Z_0, the transmission line elements can be calculated as follows

$$C_g = C_d = \frac{1}{\pi Z_o f_c} \quad (4.a)$$

$$L_g = L_d = \frac{Z_o}{\pi f_c} \quad (4.b)$$

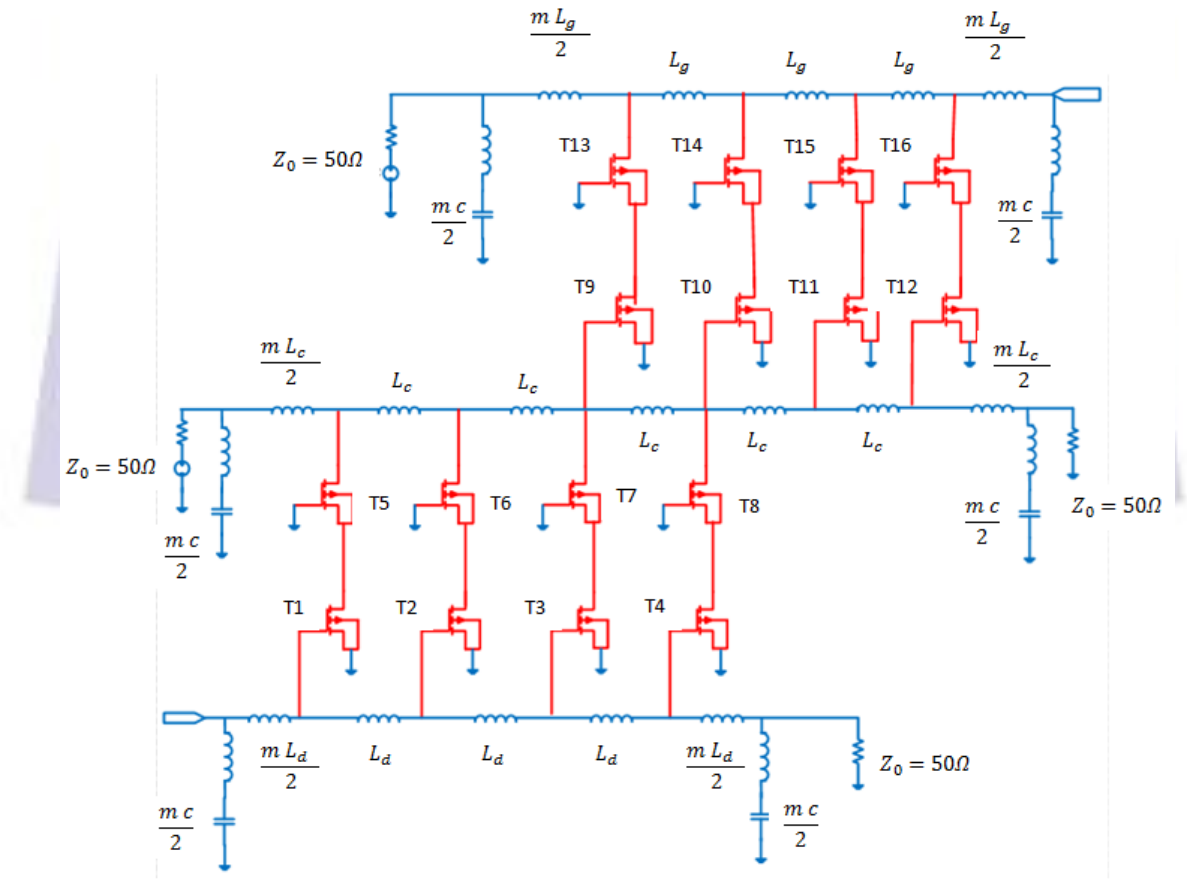
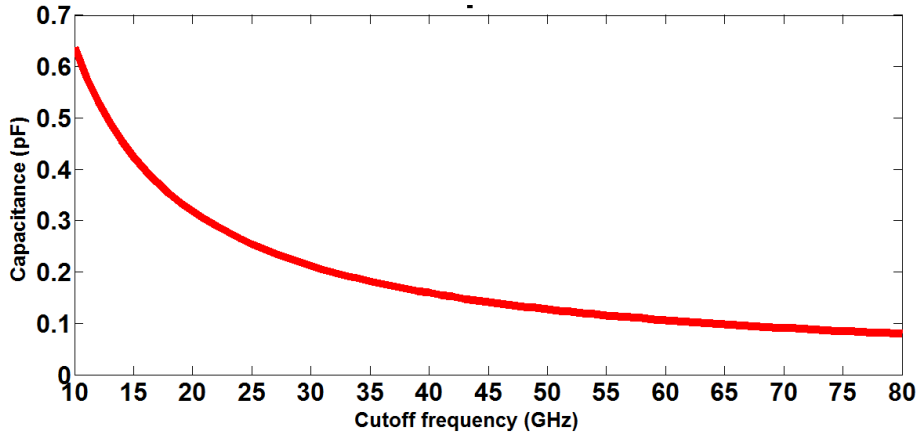
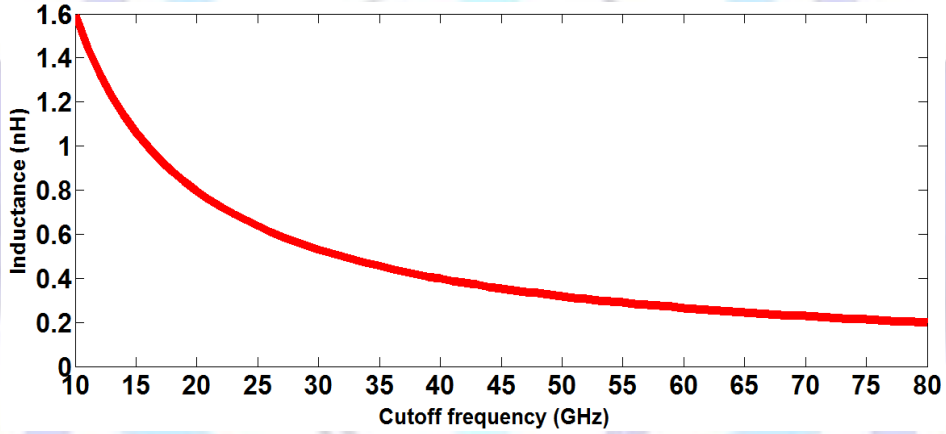


Figure 4: Circuit-level description of the proposed DA having two stages each with four amplifications cells with m-drive techniques.

Note that both capacitance and inductance are inversely proportional to the cutoff frequency f_c. This is illustrated in Figs. 5 a and b which show respectively, the dependence of $C_g = C_d$ and $L_g = L_d$ on the transmission line cutoff frequency f_c when Z_o=50 Ω. At f_c=10 GHz, $C_g = C_d$ = 0.63 pF and $L_g = L_d = 1.57$ nH. These values are to be compared with 0.08 pF and 0.19 nH for f_c=80 GHz.



(a)



(b)

Figure 5: Dependence of the transmission line capacitance (a) and inductance (b) on the cutoff frequency.

The next step is to determine transistor gate width for different submicron CMOS standards. The gate length (channel length) L is set equal to the used CMOS standard [24].The gate width is estimated using the following relation.

$$C_g = \frac{2}{3} W L C_{ox} \quad (5)$$

$$W = \frac{3 C_g}{2 L C_{ox}} \quad (6.a)$$

$$W = \frac{3}{2\pi L C_{ox} Z_o f_c} \quad (6.b)$$

where C_{ox} is the oxide capacitance per unit area. Unfortunately, values of C_{ox} for submicron CMOS standards used in this thesis <180 nm are not reported in the literature. For example, Ref. [25] gives C_{ox} for CMOS standards 800, 500, 250 and 180 nm (see Table 1). These data are curve fitted to the flowing equation

$$C_{ox} = a_2 x^2 + a_1 x + a_0 \quad (7)$$

where x is the CMOS standard in nm. The values of the fitting coefficients are

a_2 = 0.017188 $fF/mm^2.n^2\,m^2$

a_1 = -25.876 $fF/mm^2.n\,m^2$

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a_0 = 12084 fF/mm^2

Fig. 6 shows the variation of C_{ox} with CMOS standard. The marks are the data taken for Ref. [25] while the solid line denotes curve fitting. The curve fitting is used to extract C_{ox} for CMOS standards 130, 90, 65 and 45 nm (see Table 1 and Fig. 7).

Table 1: Oxide Capacitance C_{ox} for various CMOS standards.

CMOSStandard (nm)	OxideCapacitance	Referenc
800	2300	[25]
500	3800	[25]
250	5800	[25]
180	8600	[25]
130	9001	This work
90	9089	This work
65	10005	This work
45	11000	This work

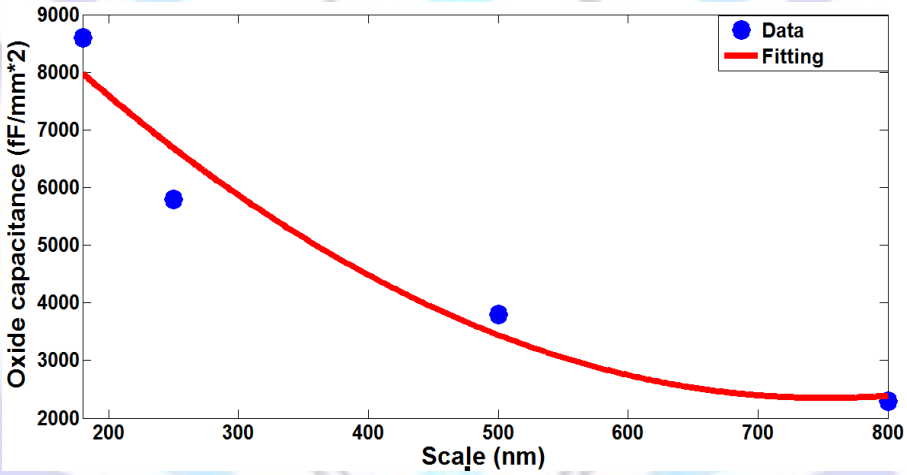


Figure 6: Variation of oxide capacitance with CMOS standard (>180 nm)

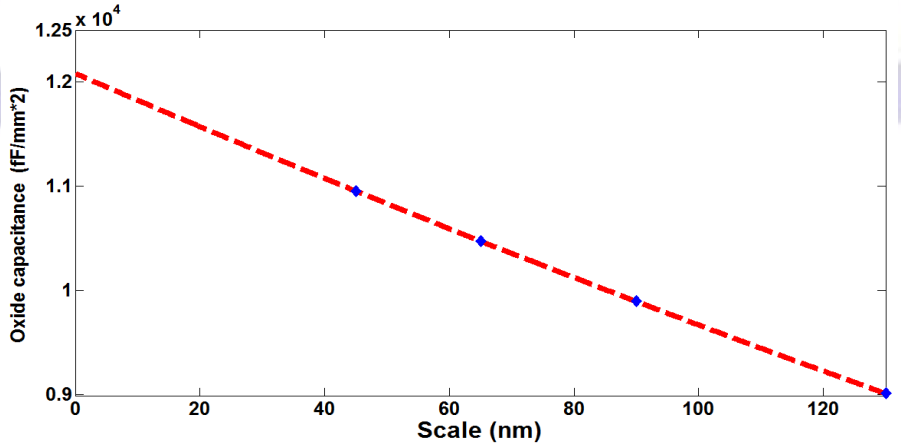


Figure 7: Extracted values of oxide capacitance for 130, 90, 65 and 45 nm standards

It is clear from Table 1 and Figs. 6 and 7 that C_{ox} increases as CMOS standard increases. This result can be explained by treating the gate capacitance simply as a two-parallel plate capacitance arises from the dioxide layer.

$C_g = \frac{A\,\varepsilon_{stox}}{t_{ox}}$ (8.a)

$C_{ox} = \frac{C_g}{A} = \frac{\varepsilon_{ox}}{t_{ox}}$ (8.b)

ε_{ox} =3.9 ε_o =3.45 x 10^{-11}F/m

where A is the gate area and ε_{ox} is the permittivity of the sillicon oxide which has t_{ox} thickness. As CMOS standard decreases, t_{ox} thickness decreases too and leading to higher values for C_{ox}.

The dependence of the gate width on the cutoff frequency of the transmission line is reflected in Equ. 6b. For a given CMOS standard, the gate width is inversely proportional to the cutoff frequency. This relation is illustrated graphically in Fig. 8 where the gate width is plotted versus cutoff frequency for different values of CMOS standards. According to Equ. 6b, W Increases as CMOS standard decreases.

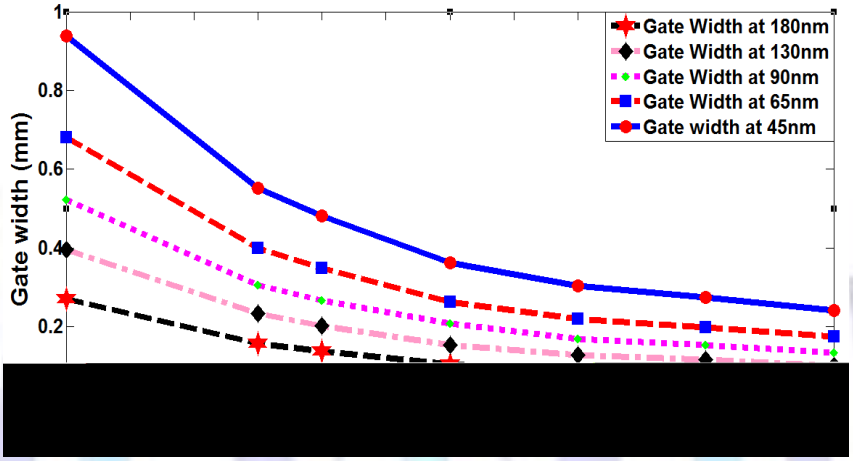


Figure 8: Dependence of gate width on transmission line cutoff frequency for different CMOS standards.

The next design step is to calculate the transistor transconductance as a function of transmission line cutoff frequency f_c for different values of CMOS standards. Recall that = ( ) when the transistor operates in the saturation region. Here is the electron mobility in the channel (assuming NMOS structure) and is the over drive voltage which is set to 0.2V in the simulation. With the aid of Equ. 6b one can arrive to the following expression for the transconductance

$$= \frac{3\,\mu_n V_{ov}}{2\,\pi L^2 Z_o f_c} \quad (9)$$

Investigating Equ. 9 reveals the following findings

I. g_m is independent of oxide capacitance C_{ox} and gate width W.

II. g_m is inversely proportion to both cutoff frequency f_c and the square of the gate length.

The electron mobility for NMOS transistors fabricated with standards 180 nm and above are reported in Ref. [25] and listed in Table 2. These data is curve fitted to the following polynomial in order to extract the values of μ_n for standards below 180 nm (see Fig. 9)

$$\mu_n = b_2 x^2 + b_1 x + b_0 \quad (10)$$

where μ_n in $cm^2/V.s$

b2= 1.7265 x$10^{-5} cm^2/V.s.n^2m^2$

b1= 0.14487 $cm^2/V.s.nm$

b0= 423.09 $cm^2/V.s$

The extracted values of μ_n for standards 130, 90, 65 and 45 nm are listed in Table 2.

Table 2: Electron mobility for various CMOS standards.

CMOS Standard (nm)	Electron Mobility ($cm^2/V.sec$)	Reference
800	550	[25]
500	500	[25]
250	460	[25]
180	450	[25]
130	442	This work
90	436	This work
65	433	This work
45	430	This work

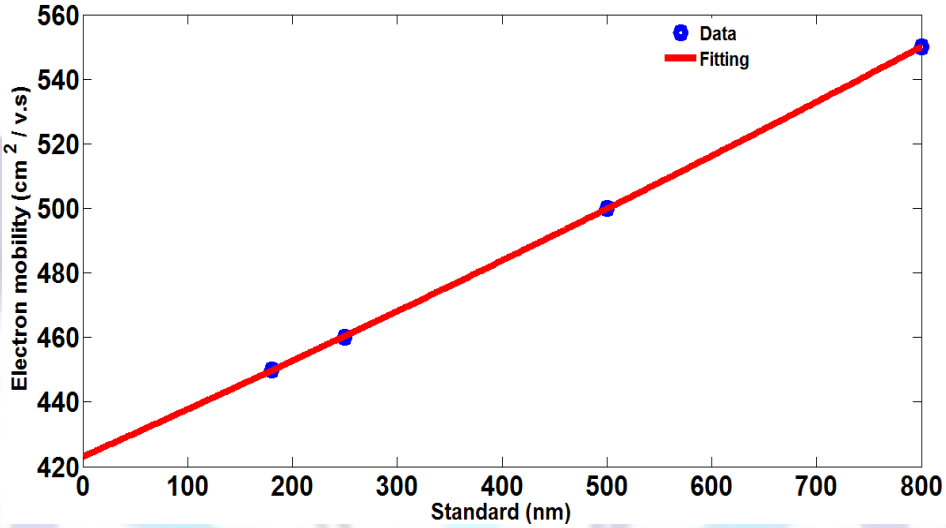
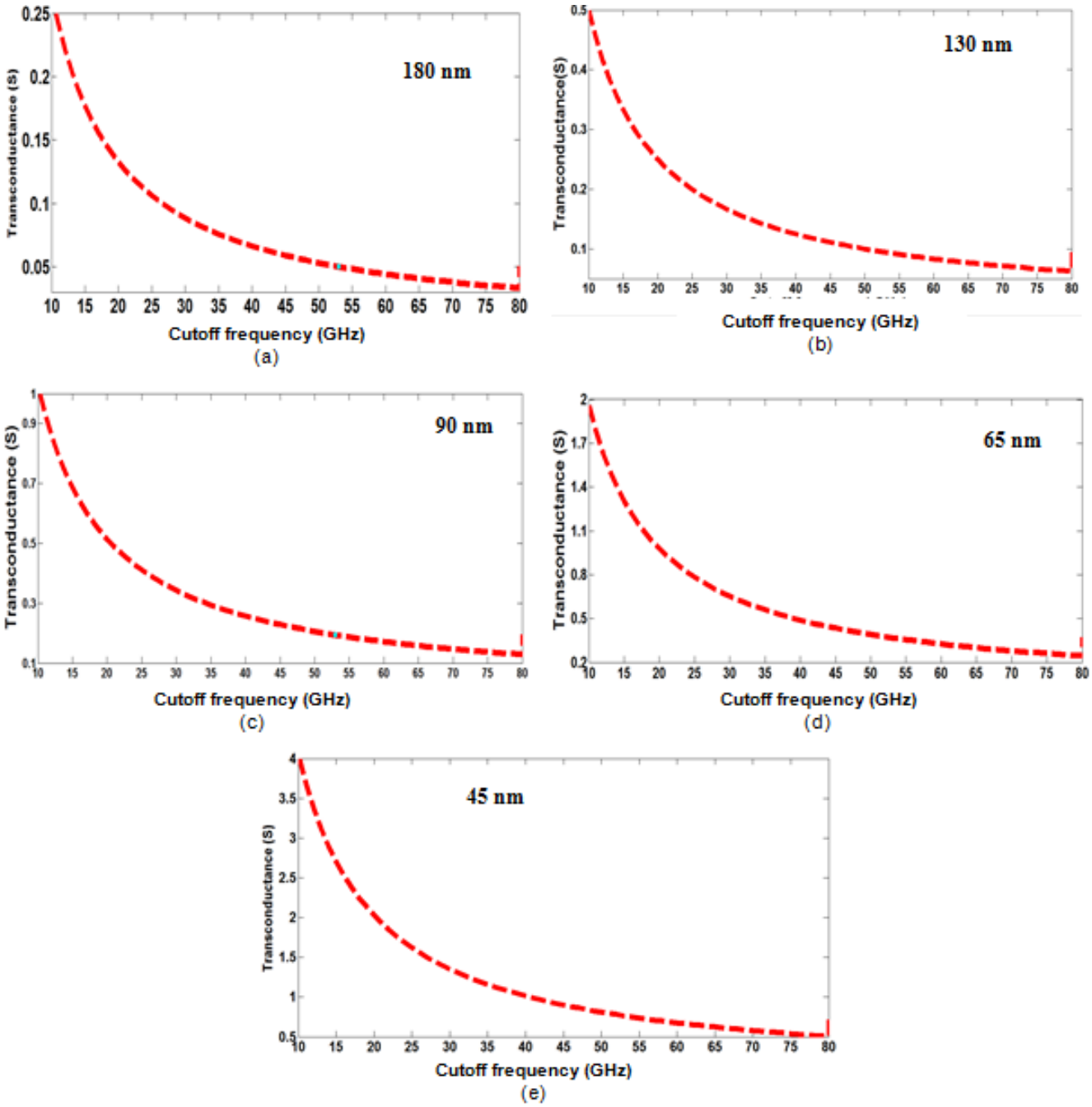


Figure 9: Variation of electron mobility with CMOS standard.

Figs. 10 a-e show the variation of transconductance with transmission line cutoff frequency for different CMOS standards 180, 130, 90, 65 and 45 nm, respectively. Note that increases rapidly as the fabrication process goes to a smaller standard. This result is expected since is inversely proportional to L^2 and the gate length L decreases as one dopted deeper submicron standards. For example, the values of at f_c = 40 GHz are 0.053S, 0.124S, 0.256S, 0.488S and 1.012S for 180, 130, 90, 65 and 45 nm standards, respectively.

Table 3 lists the required transistor design parameters (L, W and g_m) for NMOS transistor fabricated using deep submicron standards and operates at a specific value of cutoff frequency f_c.



Figuer 10: Dependence of NMOS transconductance with transmission line cutoff frequency for different standards. (a) 180 nm, (b) 130 nm, (c) 90 nm, (d) 65 nm, (e) 45 nm.

Table 3: NMOS transistor parameters for different values of cutoff frequency and fabrication standards.

Standard (nm)	Transistor Parameter	Cutoff frequency (GHz)			
		20	40	60	80
180	L (nm)	180	180	180	180
	W (μm)	270	138	87	69
	g_m (S)	0.104	0.053	0.033	0.026
130	L (nm)	130	130	130	130
	W (μm)	396	203	128	101
	g_m (S)	0.243	0.124	0.078	0.062
90	L (nm)	90	90	90	90
	W (μm)	522	267	168	134
	g_m (S)	0.500	0.256	0.161	0.128
65	L (nm)	65	65	65	65
	W (μm)	681	349	219	174
	g_m (S)	0.953	0.488	0.307	0.244
45	L (nm)	45	45	45	45
	W (μm)	939	481	303	241
	g_m (S)	1.974	1.012	0.637	0.507

4- PERFORMANCE SIMULATION RESULTS

4.1- Introduction

This section presents simulation results characterizing the gain, NF and BW of the proposed distributed amplifier for 40 and 100 Gb/s operation. The results are compared with the performance of five DA architectures, namely

I. Conventional DA which uses common-source amplification cells.
II. Cascode DA which uses cascode configuration for the amplification.
III. m-derived DA which is a conventional DA supported with both input and output m-derived stages.
IV. Matrix DA where the amplification cells are arranged in matrix-form topology.
V. Shifted second tier (SST) DA.

All the DAs considered here are designed with four amplification cells per stage. The proposed DA, matrix and SST distributed amplifiers have two stages.

Simulation results related to DA characteristic are obtained using AWR Microwave Office (version 10). The results are then used to design the proposed DA for 40 and 100 Gb/s optical receivers.

4.2- Gain and Noise Figure Spectra

The aim of this section is to investigate the gain and NF spectra when the proposed DA is designed using different nano scale CMOS technologies. The results are to be compared with other DA architectures to assess the main features behind the proposed DA.

Figs. 11 a-e illustrates the variation of the DA gains with frequency when the amplifiers are designed with 35 GHz cutoff frequency. This value of cutoff frequency is found to be suitable for operation around 40 Gb/s. Parts a-e of this figure are related to 180, 130, 90, 65 and 45 nm standards, respectively. Investigating these figures highlights the following finding. The proposed DA offers the highest gain with almost flat characteristic in the passband region compared with other DAs. Tables 4 and 5 list, respectively, the DC gain and BW of various DAs under investigation and taking the CMOS standard as independent parameter.

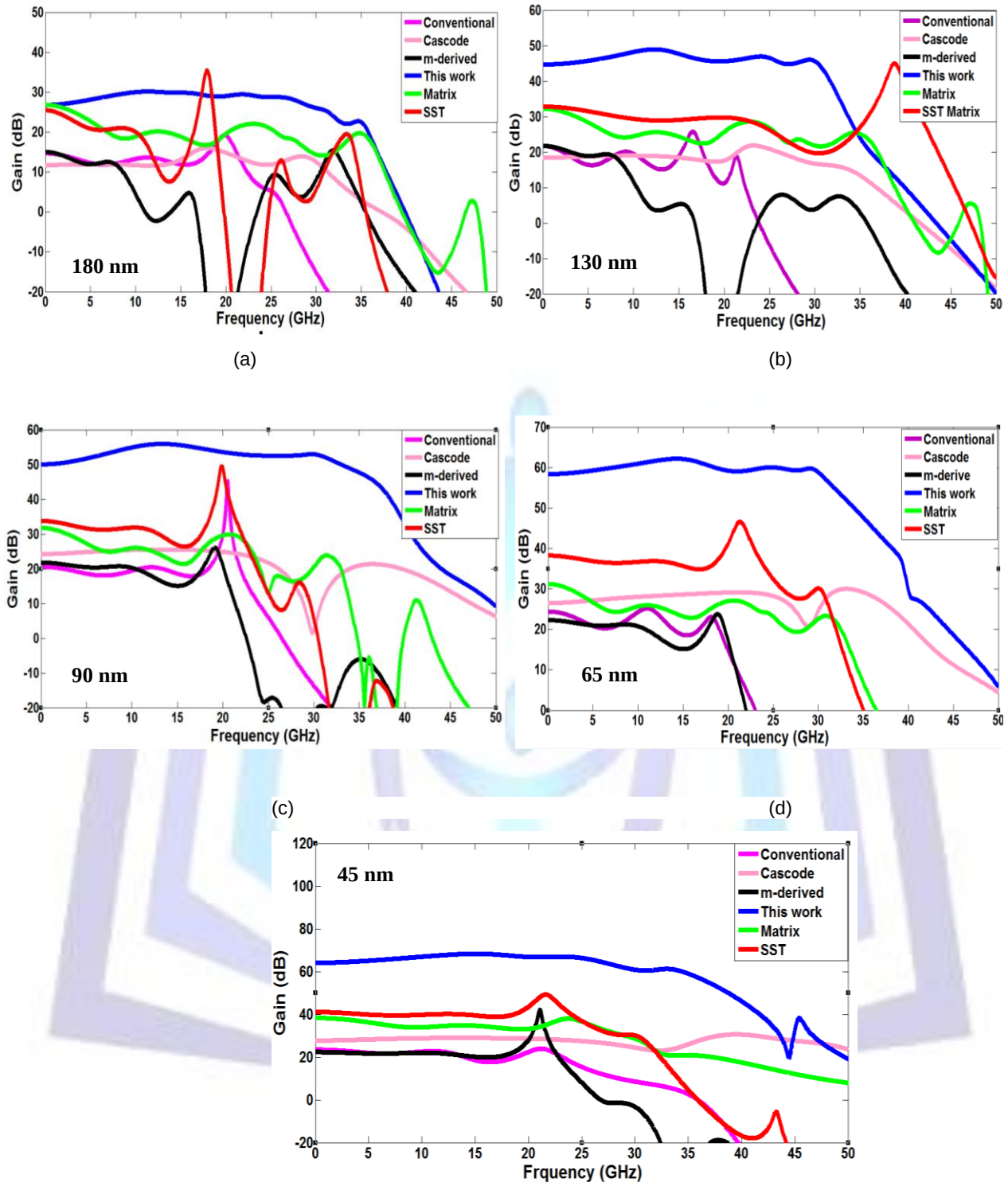


Figure 11: Gain spectra of various DA configurations designed with 35 GHz cutoff frequency using (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard, (e) 45 nm standard**.**

Table 4: DC gain of various DAs designed with 35 GHz cutoff frequency.

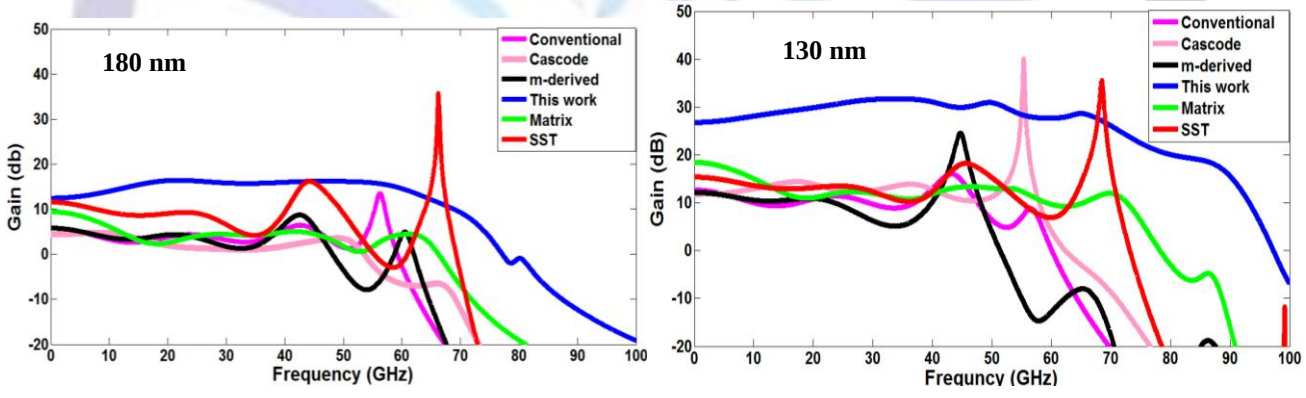
Distributed Amplifier	DC Gain (dB)				
	180 nm	130 nm	90 nm	65 nm	45 nm
Conventional	13 dB	19 dB	17 dB	20 dB	20 dB
Cascode	9 dB	15 dB	23 dB	23 dB	24 dB
m-derived	12 dB	19 dB	17 dB	19 dB	20 dB
Matrix	22 dB	27 dB	29 dB	29 dB	35 dB
Shifted second tier	21 dB	29 dB	33 dB	33 dB	39 dB
This work	24 dB	42 dB	47 dB	56 dB	62 dB

Table 5: Bandwidth of various DAs designed with 35 GHz cutoff frequency.

Distributed Amplifier	Bandwidth (GHz)				
	180 nm	130 nm	90 nm	65 nm	45 nm
Conventional	1.2 GHz	3 GHz	6 GHz	5 GHz	6 GHz
Cascode	30 GHz	32 GHz	26 GHz	28 GHz	29 GHz
m-derived	7 GHz	8 GHz	11 GHz	10 GHz	19 GHz
Matrix	3.7 GHz	4 GHz	5 GHz	5.5 GHz	7 GHz
Shifted second tier	9.7 GHz	20 GHz	13 GHz	16 GHz	18 GHz
This work	31 GHz	31 GHz	34 GHz	32 GHz	34 GHz

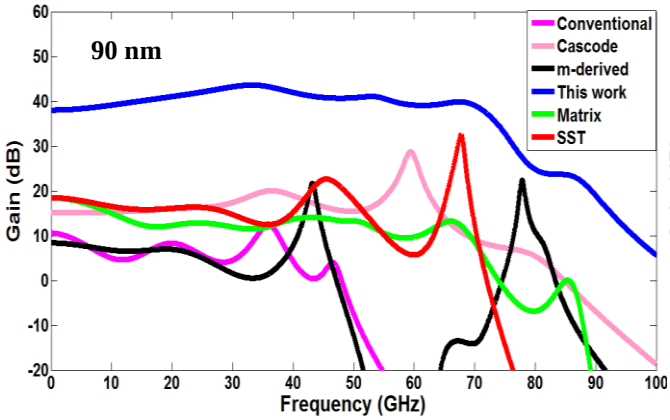
From the results illustrated in Fig. 11 and Tables 4 and 5 one can find out that the proposed DA the best results (highest gain and BW) when compared with other DAs. Conventional DA gives medium gain but not flat with low BW. Cascode DA gives low gain with BW range close to this work. M-derived DA gives flat medium gain with low BW. Matrix DA gives high gain but not flat with low BW. SST gives flat high gain with low BW.

The simulation is repeated to investigate the characteristics of 80 GHz-cut off frequency DAs suitable for around 100 Gb/s operation. The results are presented in Fig. 12 to highlight the gain spectrum and summarised in Tables 6 and 7 to assess the DC gain and BW, respectively, of various DAs synthesized with nanoscale CMOS standards.

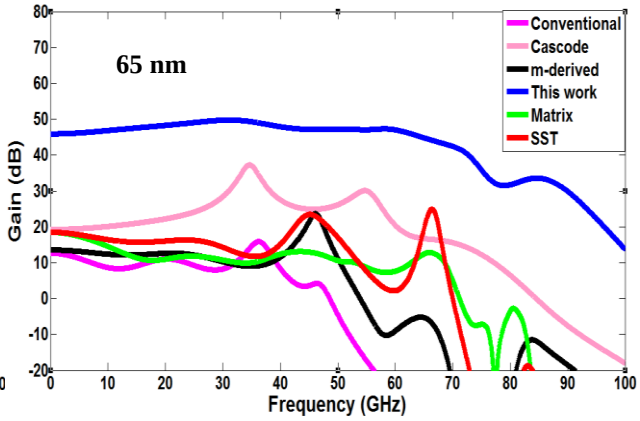


(a) (b)

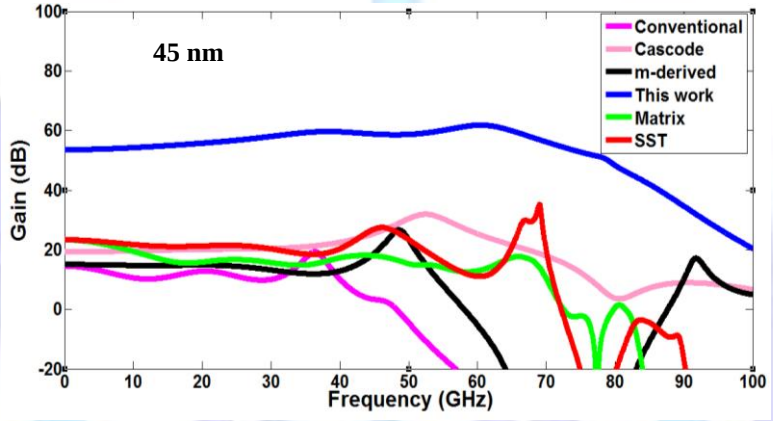
Figure12: Gain spectra of various DA configurations designed with 80 GHz cut off frequency using (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard, (e) 45 nm standard**.**



(c)



(d)



(e)

Figure12: (Continued)

Table 6: DC gain of various DAs designed with 80 GHz cutoff frequency.

Distributed Amplifier	DC Gain (dB)				
	180 nm	130 nm	90 nm	65 nm	45 nm
Conventional	3 dB	9 dB	9 dB	9 dB	11 dB
Cascode	2 dB	8 dB	12 dB	15 dB	17 dB
m-derived	3 dB	8 dB	8 dB	10 dB	12 dB
Matrix	6 dB	15 dB	15 dB	15 dB	19 dB
Shifted second tier	9 dB	12 dB	14 dB	15 dB	20 dB
This work	10 dB	23 dB	34 dB	42 dB	49 dB

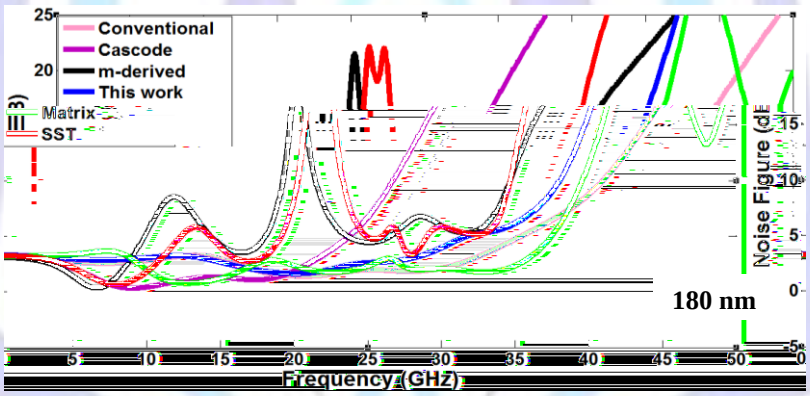
Table 7: Bandwidth of various DAs designed with 80 GHz cutoff frequency.

Distributed Amplifier	Bandwidth (GHz)				
	180 nm	130 nm	90 nm	65 nm	45 nm
Conventional	19 GHz	20 GHz	16 GHz	17 GHz	12 GHz
Cascode	50 GHz	52 GHz	59 GHz	63 GHz	68 GHz
m-derived	27 GHz	28 GHz	25 GHz	29 GHz	35 GHz
Matrix	10 GHz	10 GHz	9 GHz	9 GHz	13 GHz
Shifted second tier	27 GHz	31 GHz	32 GHz	30 GHz	58 GHz
This work	70 GHz	75 GHz	74 GHz	71 GHz	75 GHz

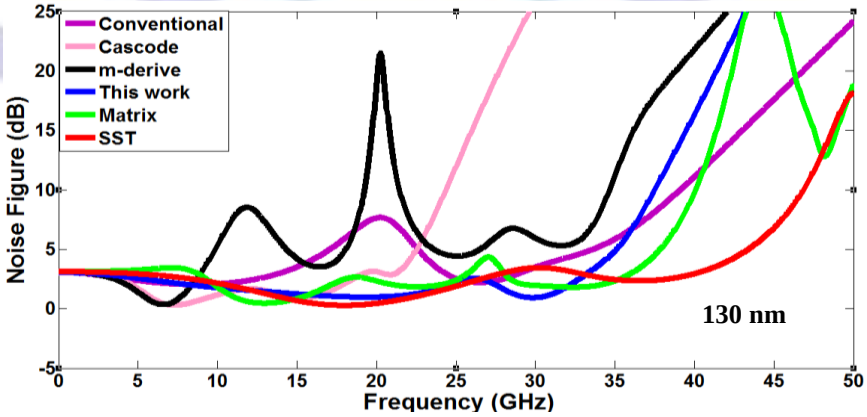
Investigating the results in Fig 12 and Tables 6 and 7 reveals that the same conclusions drawn from the 35 GHz cutoff frequency DAs are also applied.

The results also show that when the cutoff frequency increases, the gain decreases for all DAs. However, the proposed DA gives the highest gain. One can apply these results to all standards (180, 130, 90, 65 and 45 nm).

The simulation is carried further to assess the NF spectrum of 35 GHz – and 80 GHz cut off frequency DAs and the results are displayed in Figs. 13 and 4.4, respectively. Tables 8 and 9 summarises the dependants of low frequency NF on CMOS standard for various DA configurations.

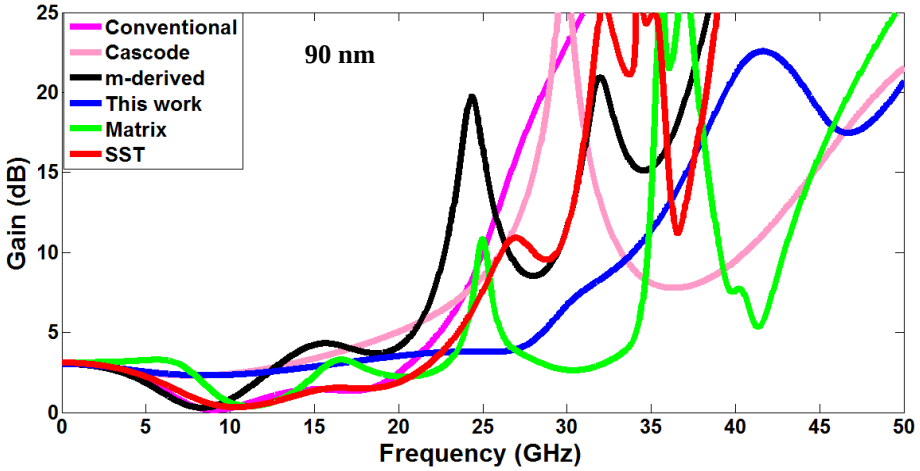


(a)

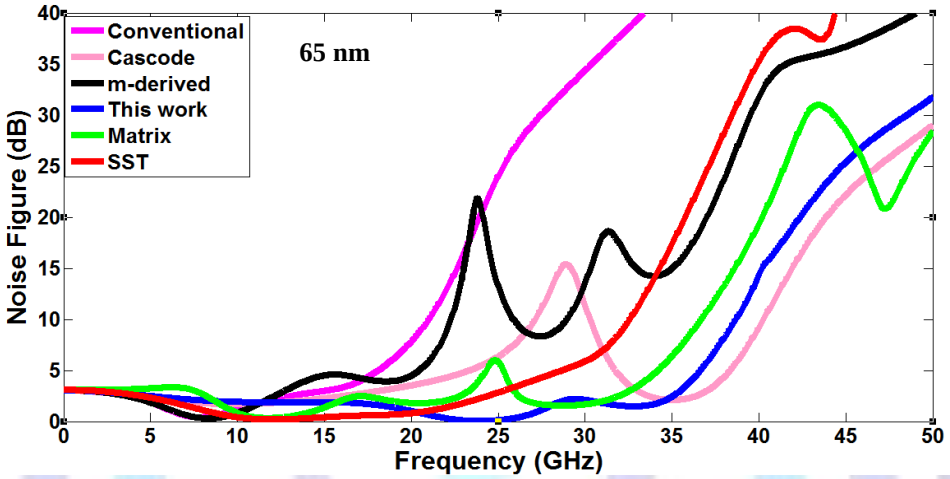


(b)

Figure13: Noise figure spectra of various DA configurations designed with 35 GHz cutoff frequency using (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard, (e) 45 nm standard.



(c)



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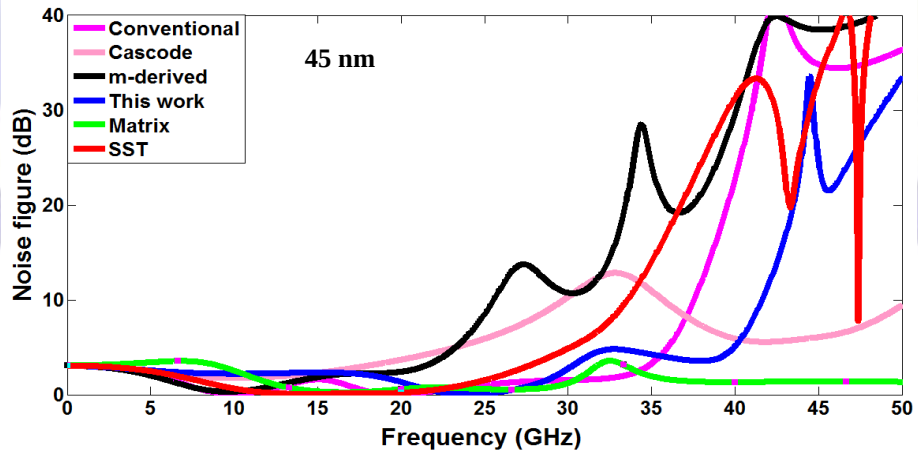

(e)

Figure13: (Continued)

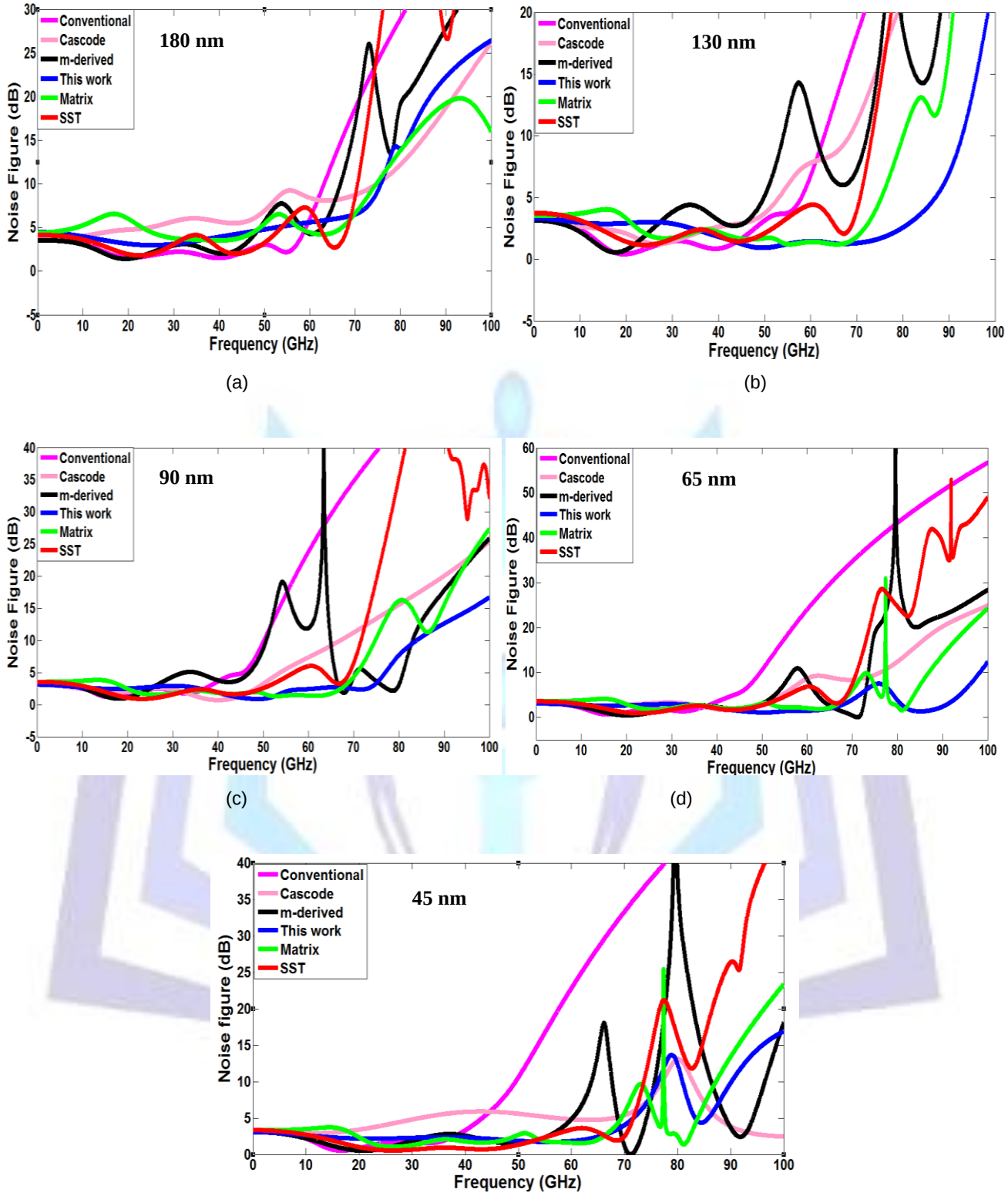

Figure14: Noise figure spectra of various DA configurations designed with 80 GHz cutoff frequency using (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard, (e) 45 nm standard.

Table 8: Noise figure of various DAs designed with 35 GHz cutoff frequency.

Distributed Amplifier	DC Noise figure (dB)				
	180 nm	130 nm	90 nm	65 nm	45 nm
Conventional	3 dB	4 dB	16 dB	30 dB	3 dB
Cascode	15 dB	25 dB	14 dB	10 dB	9 dB
m-derived	5.1 dB	4.5 dB	8 dB	18 dB	1.7 dB
Matrix	2.4 dB	2.2 dB	3.7 dB	2.2 dB	4 dB
Shifted second tier	3 dB	3.6 dB	10 dB	5 dB	2 dB
This work	4 dB	1.5 dB	5 dB	1.7 dB	2 dB

Table 9: Noise figure of various DAs designed with 80 GHz cutoff frequency.

Distributed Amplifier	DC Noise figure (dB)				
	180 nm	130 nm	90 nm	65 nm	45 nm
Conventional	18 dB	12 dB	26 dB	30 dB	36 dB
Cascode	7 dB	7.3 dB	10.1 dB	8 dB	5 dB
m-derived	18 dB	5 dB	0.8 dB	1 dB	0.3 dB
Matrix	2.5 dB	2.5 dB	1.5 dB	4 dB	2 dB
Shifted second tier	2 dB	3 dB	3 dB	4.5 dB	4 dB
This work	6 dB	1.7 dB	3 dB	3.5 dB	3.5 dB

From the results illustrated in Figs. 5 and 6 and Tables 8 and 9 one can find out that proposed DA gives low NF with almost flat spectrum when compared with other DAs. The value of the NF of this DA doesn't exceed 6 dB for all standards (180, 130, 90, 65 and 45 nm).

4.3- Effect of Transmission Line Cutoff Frequency

The cutoff frequency f_c of drain and gate transmission lines is usually used as one of the main entry design parameters for DAs. This section illustrates the depends of DA characteristic on the cutoff frequency. The results are reported for various DA architectures and various CMOS standards. The investigation is focused on low-frequency gain, low-frequency NF, and 3 dB BW.

Figs. 15 a-e shows the dependence of the low-frequency gain on the line cutoff frequency for CMOS standards 180, 130, 90, 65 and 45 nm, respectively. Note that the proposed DA has the highest gain among the DAs considered here and this conclusion holds true for all cutoff frequency and CMOS standards. Note further that the amplifier gain decreases as the cutoff frequency increases.

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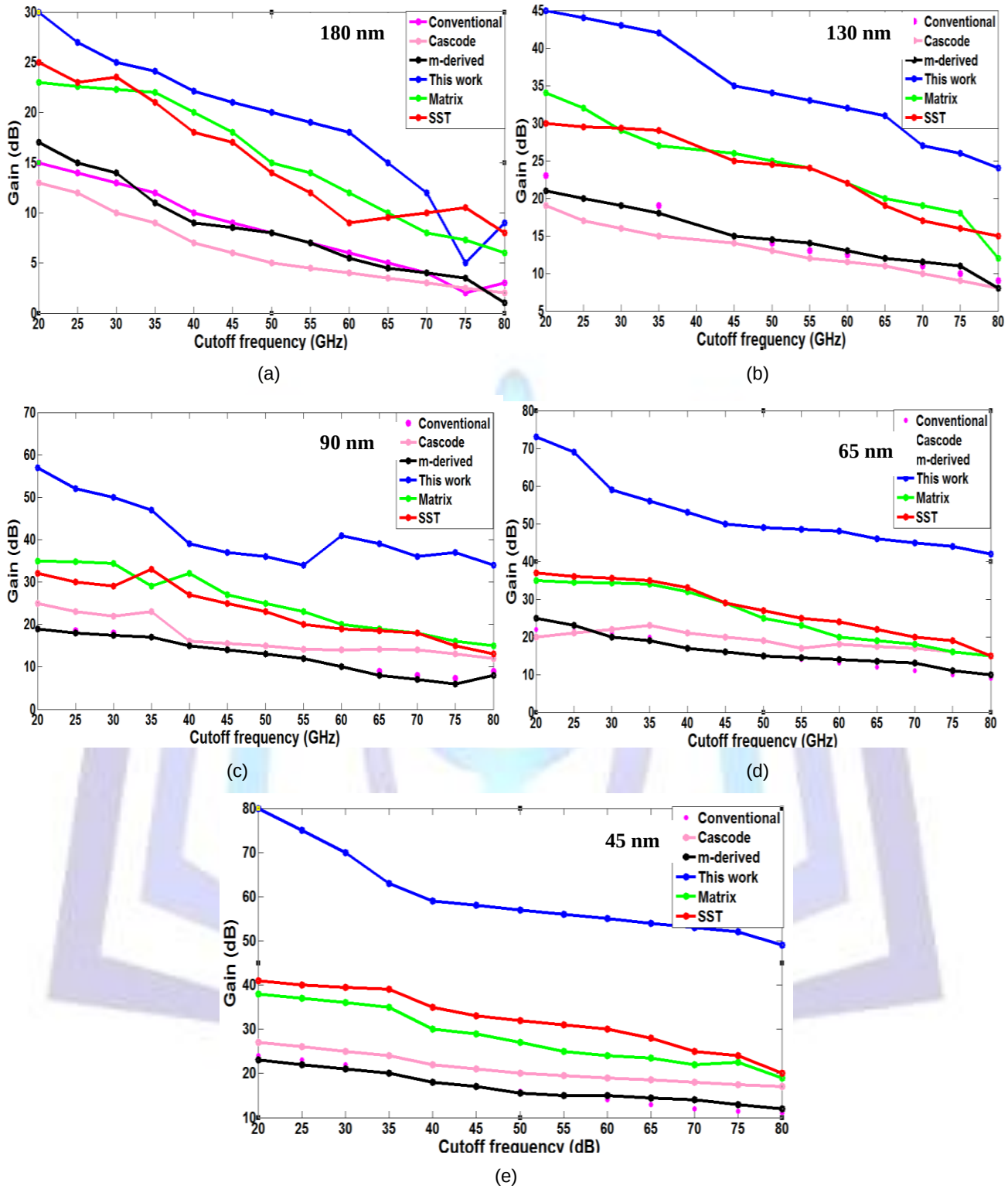


Figure15: Dependence ofgain on cutoff frequency for various DAs designed using CMOS technology of (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard and (e) 45 nm standard.

Variation of low-frequency NF with cutoff frequency is given in Fig. 16. The results are reported for various DA configuration and CMOS standards. Investigation the results in this figure highlights the following findings. The proposed DA is characterized by relatively low NF over all values of cutoff frequency and CMOs standards.

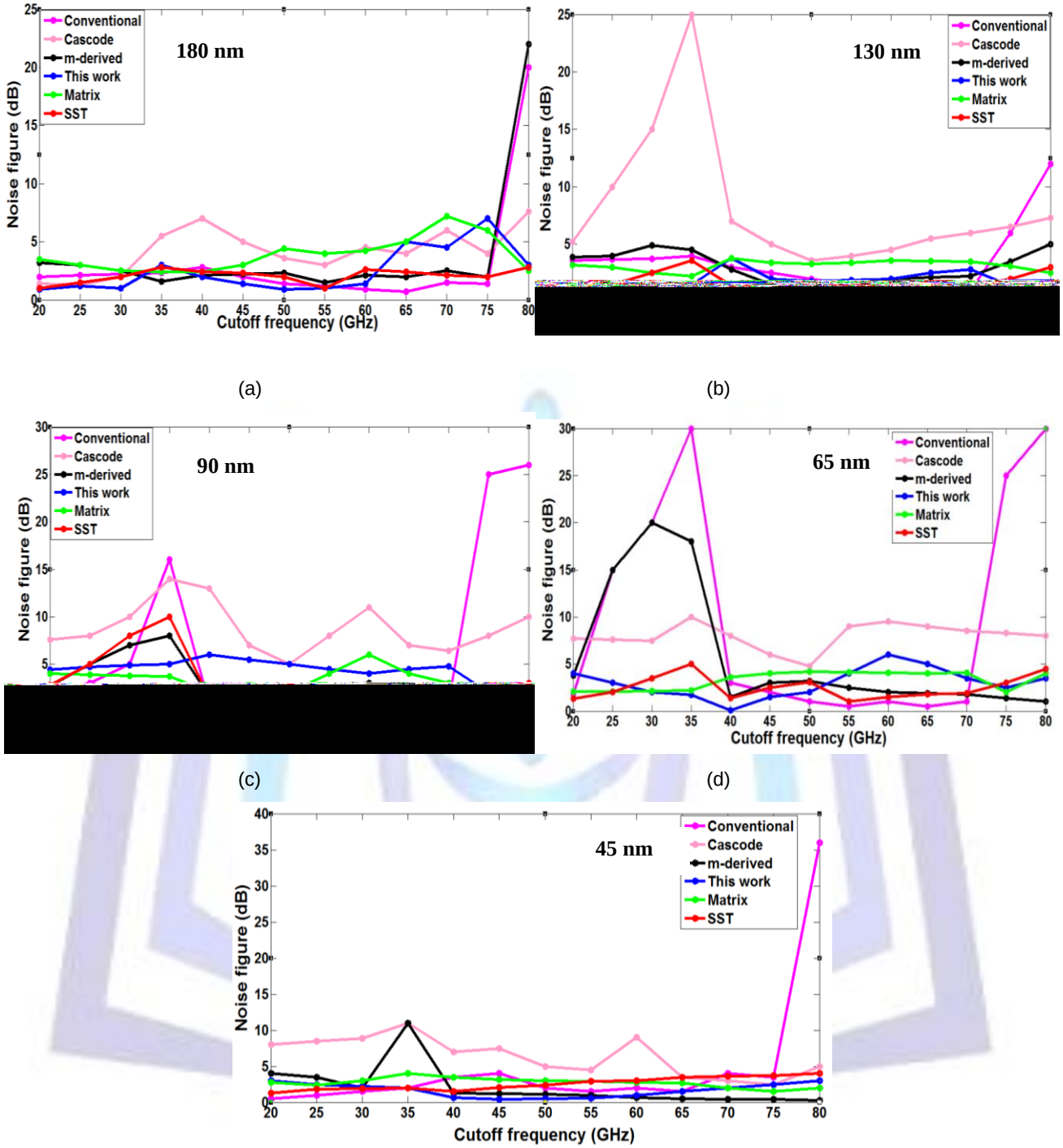


Figure16: Dependence ofnoise figure on cutoff frequency for various DAs designed using CMOS technology of (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard and (e) 45 nm standard.

The calculation is carried further to estimate the 3 dB BW of the DAs and the results are displayed in Fig. 17 for various CMOS standards. The main conclusions drawn from this figure are

I. For a given cutoff frequency, the proposed DA generally offers the highest BW compared with other DAs and this effect is more pronounced for high CMOS standards. For example, at 35 GHz cutoff frequency and 180 nm standard, the BWs of the proposed, cascode, SST, m-derived, matrix and conventional DAs are 31, 30, 9.7, 7, 3.7 and 1.2 GHz, respectively. These values are to be compared with 31, 31, 10, 8, 4 and 3 GHz for 130 nm DAs designed with 35 GHz cutoff frequency.

II. In general, the BW of all DAs increases with cutoff frequency and this effect is more pronounced with the proposed DA. For example, if the DAs are designed with f_c = 80 GHz and 180 nm standard, then the BW are

enhanced by 2.25, 1.66, 2.7, 3.85, 2.70 and 15.83 for the proposed, cascode, SST, m-derived, matrix and conventional DAs when compared with 35 GHz cutoff frequency counterparts.

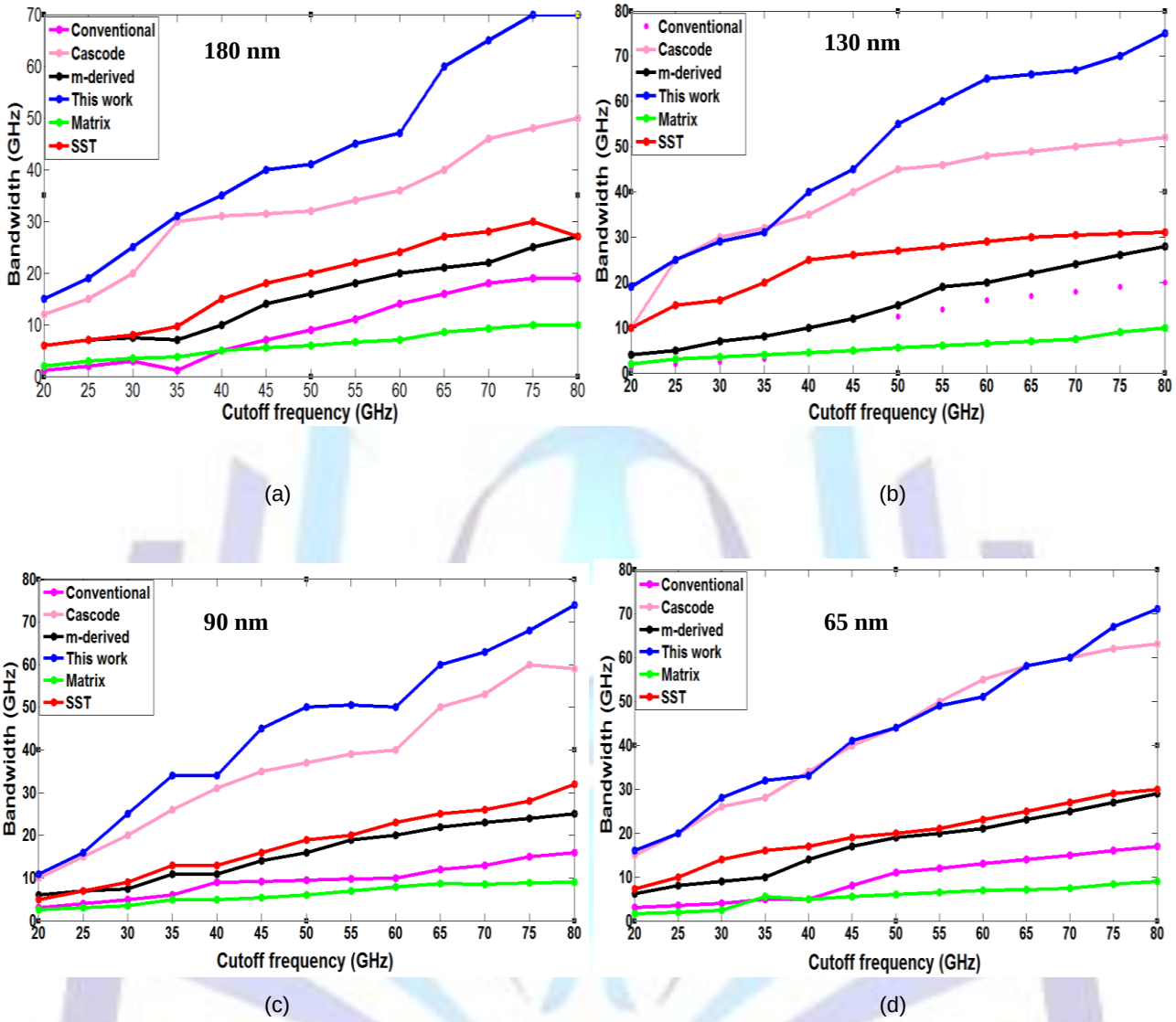
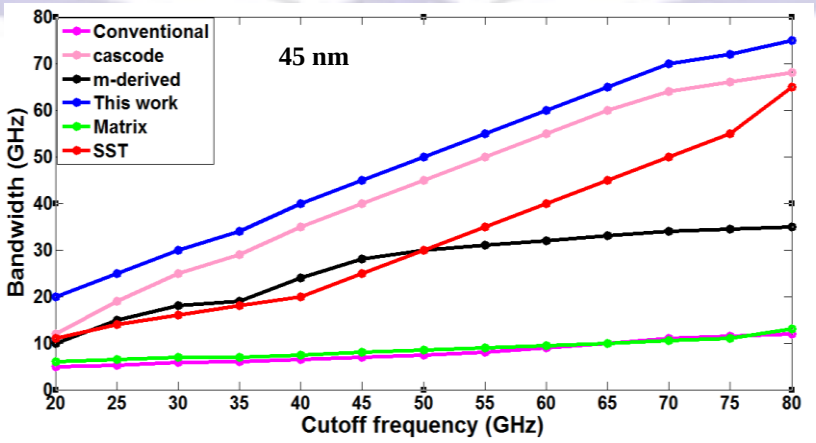


Figure17: Dependence ofbandwidth on cutoff frequency for various DAs designed using CMOS technology of (a) 180 nm standard, (b) 130 nm standard, (c) 90 nm standard, (d) 65 nm standard and (e) 45 nm standard.



(e)

Figure17: (Continued)

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4.4- Designing the Proposed DAs for 40 and 100 Gb/s Operation

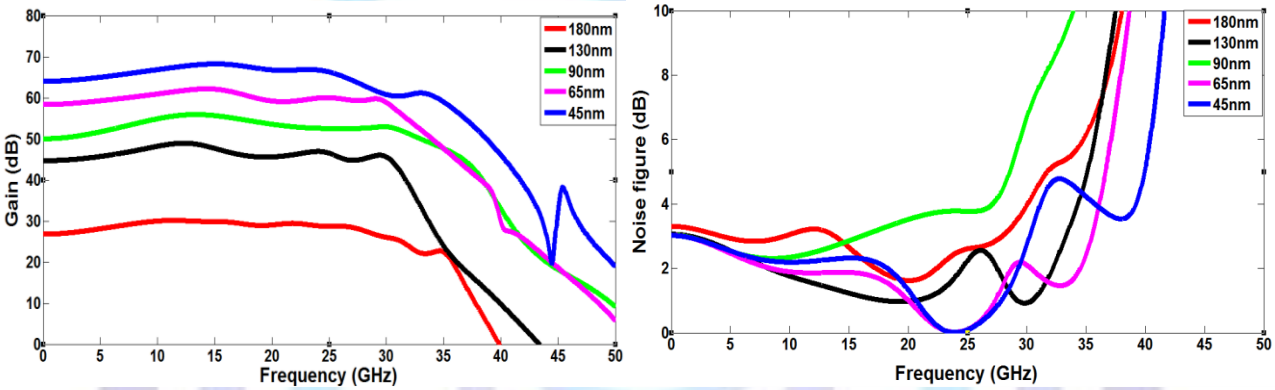
The results reported in the previous sections can be used as a guideline to design the proposed DA for front-end amplification in 40 Gb/s and 100 Gb/s optical receivers. The BW of the optical receiver is usually set equal to 0.7x bit rate as a hand of thumb estimate.

From Fig. 17, one can deduced the cutoff frequencies for various CMOs standards that can be used as a design parameter to achieve BWs corresponding to 40 and 100 Gb/s. This design parameter is used to deduce both geometric and characteristics parameters of the DAs. Tables 10 and 11 list the obtained results, for both 40 and 100 Gb/s DAs, respectively. Again various CMOS standards are used to estimate the DA parameters for both operating bit rates. The thickness of the oxide layer t_{ox} is calculated from the gate capacitance using a simple model based on parallel-plate capacitance,

$$t_{ox} = \frac{\varepsilon_{ox}}{C_{ox}} \quad (11.a)$$

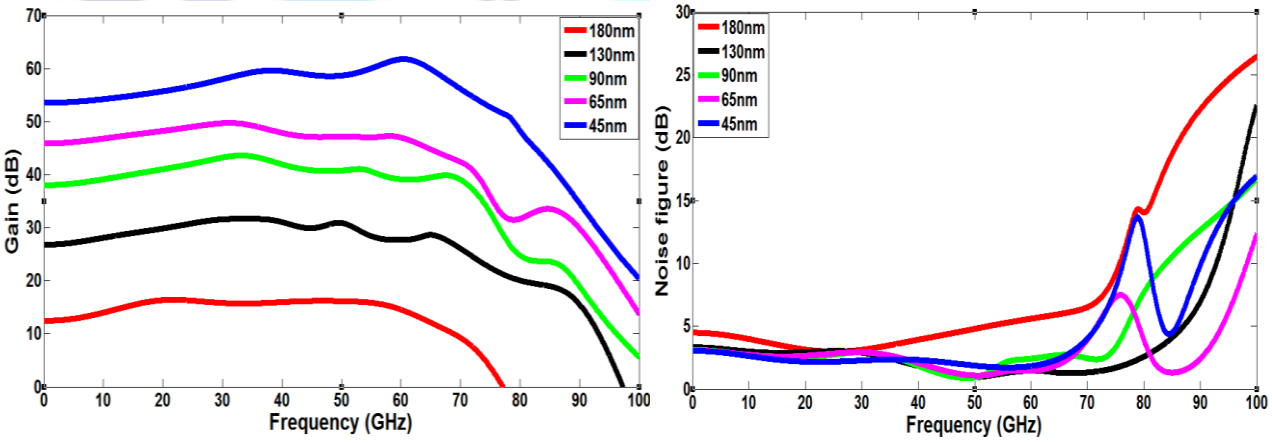
ε_{ox} =3.9 ε_o =3.45 x 10^{-11}F/m (11.b)

Figs. 18a and 18b show the gain and NF spectra for 40 Gb/s DAs designed with different CMOS standards. The calculations are repeated in Figs. 19a and 19b for the designed 100 Gb/s DAs.



(a) (b)

Figure 18: Gain and noise figure spectra for the proposed 40 Gb/s DA designed using different CMOS standards.



(a) (b)

Figure 19: Gain and noise figure spectra for the proposed 100 Gb/s DA designed using different CMOS standards.

Table 10: Design and characteristics parameters of the proposed DA for 40 Gb/s operation. Cutoff frequency of 35 GHz is used in the design.

Parameter	Value				
	180 nm	130 nm	90 nm	65 nm	45 nm
Gate length (nm)	180	130	90	65	45
Gate width (μm)	158	233	306	399	551
Oxide thickness (nm)	4	3.8	3.7	3.4	3.1
Transconductance (S)	0.061	0.142	0.293	0.559	1.159
Gain (dB)	25	42	47	59	62
Noise figure (dB)	3	1.5	3.5	1.7	2
Gain - BandwidthProduct (GHz)	551	3902	7611	28512	42772

Table 11: Design and characteristics parameters of the proposed DA for 100 Gb/s operation. Cutoff frequency of 80 GHz is used in the design.

Parameter	Value				
	180 nm	130 nm	90 nm	65 nm	45 nm
Gate length (nm)	180	130	90	65	45
Gate width (μm)	69	101	134	174	241
Oxide thickness (nm)	4	3.8	3.7	3.4	3.1
Transconductance (S)	0.026	0.062	0.128	0.244	0.507
Gain (dB)	10	23	34	42	49
Noise figure (dB)	6	1.2	3	3.5	3.5
Gain x Bandwidth Product (GHz)	221	1059	3708	8938	21137

From the results illustrated in graphs and tables above, one can find that the gain is increased by increasing the standard values, this can applied at both 35 and 80 GHz cutoff frequency, and the value of NF remains low. Gate width also increased by increasing the standard values, oxide thickens decrease by increasing the standard value, while transconductance increase by increasing standard value.

5- CONCLUSIONS

A new distributed amplifier architecture has been introduced to achieve high flat gain and low noise figure over ultra wideband bandwidth. Investigation has been carried out to assess the performance of the proposed DA when it is implemented in various submicron CMOS standards process. The results have been used to design DAs for front-end amplification in 40 and 100 Gb/s optical receivers. The main conclusions drawn from this work are

I. The proposed DA offers the highest gain among various DAs investigated in this work.

II. The proposed DA offers a nearly flat gain over the wide bandwidth. The degree of gain flatness is the highest among the investigated DAs.

III. Designing the DAs with high cutoff frequency leads to gain reduction.

IV. The noise figure of the proposed DA does not exceed 6 dB for various CMOS standards.

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