



## Nand gate architectures for memory decoder

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### ABSTRACT

This paper presents some nand gate design styles which when used in decoder reduces energy consumption and delay. Basically conventional, nor style nand, source coupled nand is discussed. The three designs conventional, nor style nand, source coupled nand, ranges in area, speed and power. In nor style nand transistors are added in parallel so high fan-in is obtained and logical effort is reduced. In source coupled nand number of transistors are reduced it give speed of operation compared to an inverter. When simulated and compared it is found that nor style nand is 35% faster and 67 % more power efficient than conventional. Source coupled nand is found to be 36% faster and 82% more power efficient than conventional nand gate

### Indexing terms/Keywords

Memory decoder, nor based nand, source coupled nand, high speed, low power.

### Academic Discipline And Sub-Disciplines

Electronics and communication ,VLSI design.

### SUBJECT CLASSIFICATION

High speed and low power circuit design, memory design.

### TYPE (METHOD/APPROACH)

All the architectures are simulated and verified on CADENCE tool using 0.18 um technology,level 53 model file. For schematic entry cadence composer is used, for simulation Cadence Spectre 5.1.4 1\_ISR , for layout Cadence Virtuoso 5.1.4 1\_ISR is used and its DRC, LVS and RCX is done using Cadence Assura 3.2.0.

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## INTRODUCTION

In most of the memory systems memory modules are widely used. According to ITRS (international technology roadmap for semiconductor), the memory chip will occupy 90% of the chip area by 2013. In many systems like microprocessors memory is accessed repeatedly and very high performance systems do this every clock cycle. The clock network power consumption due to memory devices ( i.e. Cache memory, registers) account of 51% of total power [1]. This generates a need to study schemes/methods to reduce power dissipation in memories. Fig.1 shows a basic block diagram of memory system.

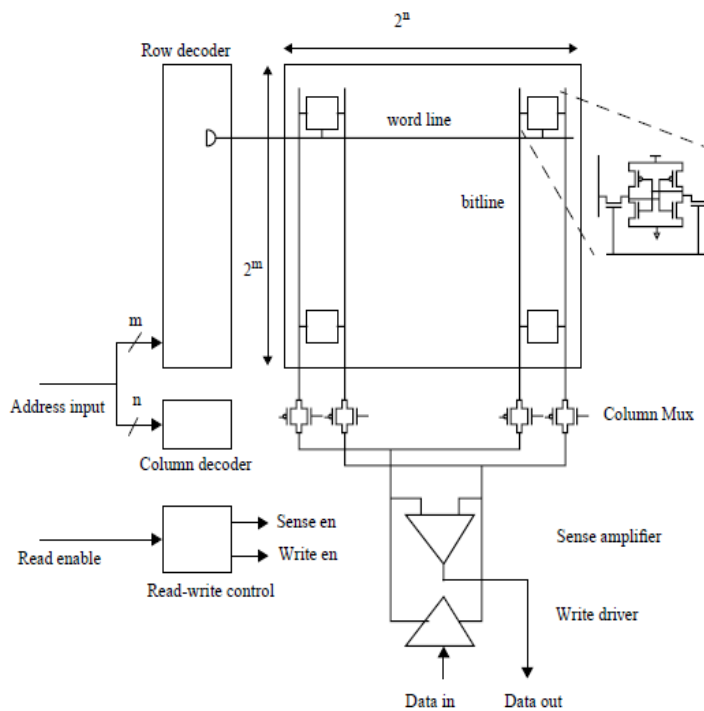


Fig 1: block diagram of memory system

In this power dissipation can be reduced by optimizing SRAM cell, by optimizing sense amplifier and also the bit line. But there is not so much research on making memory decoder efficient for speed and power. Decoder is used to select a word line based on the input address. It basically consists of and gates. So by optimizing that gate the speed and power performance of decoder can be improved.

This paper presents the various circuit styles conventional, nor style nand, source coupled nand which reduces area, selectively precharge some select lines so minimize power dissipation and also gives improved performance in terms of speed when compared to conventional means.

### Conventional nand gate:

As the two n-fets are connected in series stack form. So to obtain the same drive capability as that of inverter the n-fets should be twice as big as in an inverter. But in submicron technology because of velocity saturation in inverter fet its current is not as twice as that of series stack. For 180nm technology it is found that the same current drive capability is obtained with n-fet in series stack is 1.2 times larger than inverter n-fet[2]. In decoders based on conventional gates one of the output is asserted based on the input address. For next address input the previous output first has to be deasserted and the new decoder output has to be asserted. This operation reduces the speed. The above problem can be overcome by using pulsed decoder[3], in which output stays active for a minimum time and then shuts off. In this gates used are conventional but input is given in the form of pulses of short duration. So before any access all the word lines are off is to be guaranteed. So decoder needs to activate one of the word lines.

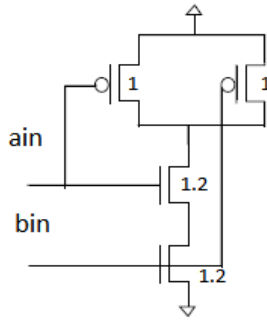


Fig 2(a): conventional nand gate

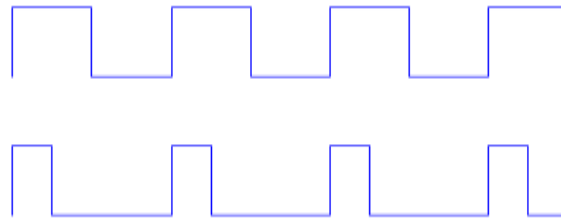


Fig 2(b): difference between conventional input and pulsed input

**Nakamura nand gate:**

In this PMOS size is halved that of conventional. This does not effect rise time because it is guaranteed that the inputs will be deasserted. This will make the decoder faster than above two styles.

Problem in all of the above design styles is that if we are using 3 input, 4 input or more input gate then charge sharing between output node and the intermediate node capacitance become significant which may degrade the performance and may cause erroneous outputs. Depending upon the value of internode capacitance the charge at output node can fall up to  $(V_{dd}/2)$ . So depending on threshold value '1' at output will become '0'.

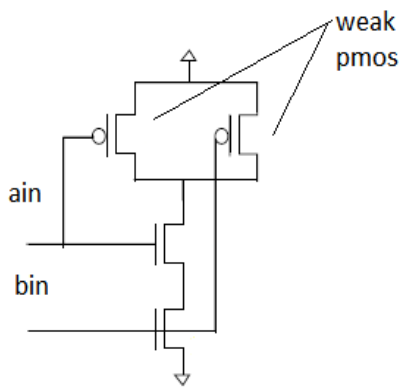


Fig.3(a) nakamura nand gate

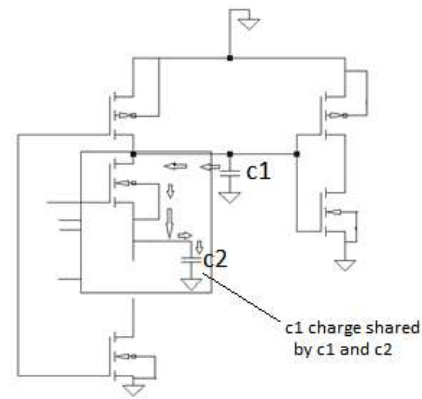


Fig.3(b) representing charge sharing problem

Adding a weak PMOS improve the performance but transistor count increases.

**Nor style nand gate:**

As the fan-in of nor gate is very large in domino circuits. A large fan-in nand can be implemented doing a nor of the complementary inputs and it is very good option for designing high speed decoders.

In this as the number of inputs increases the n-fets are added in parallel. So internode capacitance does not form and charge sharing is not a problem in this technique. When clock goes low both nodes precharge high. When clock goes high the behavior of circuit depends on the applied inputs. If any one or more inputs are high then node A will discharge so transistor M gets off [4].

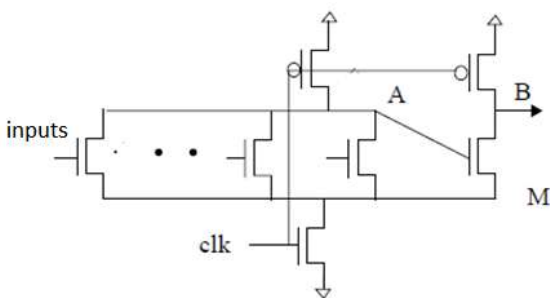


Fig 4(a): n-input nor style nand gate[4]

In1	In2	In1b	in2b	output
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Fig 4(b): truth table of 2 input nor style nand gate

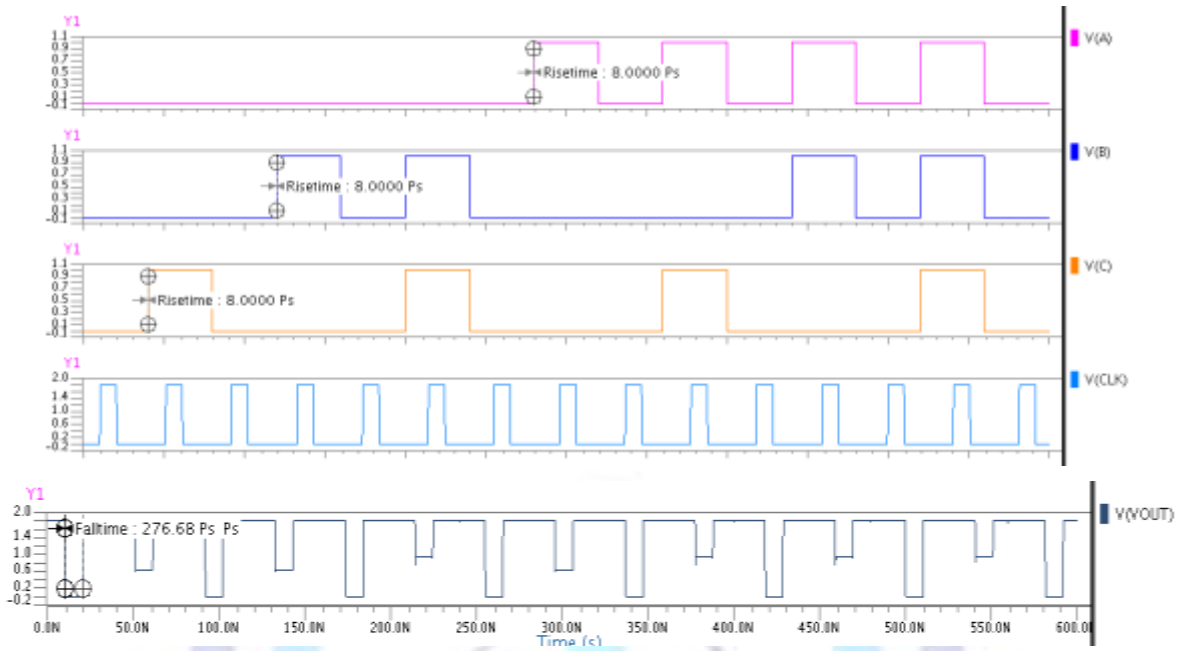


Fig 4(c): output waveforms for nor style nand gate

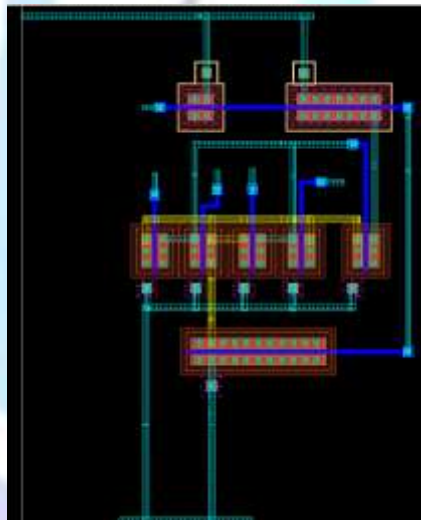


Fig 4(d): showing the layout of a 4-inputs nor style nand gate

But the discharging of node A should be fast otherwise the high level at output will be degraded and output may become false. As the number of inputs increases the numbers of transistors used are also less than that of conventional style.

**Source coupled nand style:**

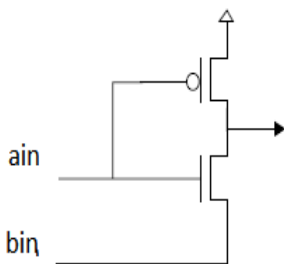


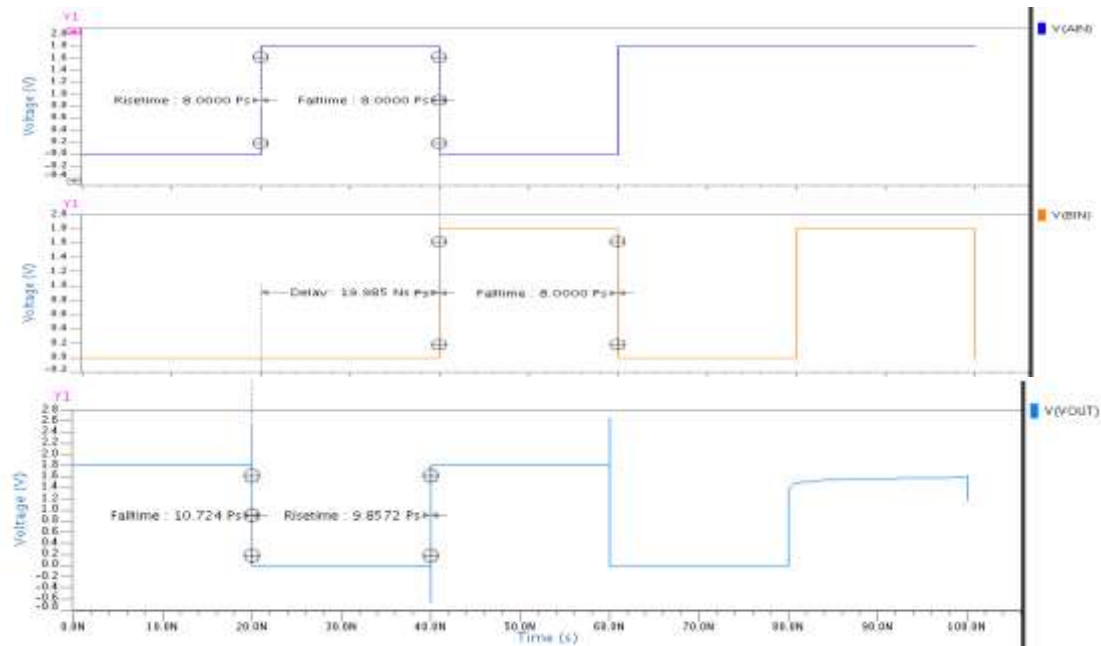
Fig 5(a): source coupled nand gate

one of the most efficient style of designing a decoder both in terms of speed and power dissipation. Up to 4 inputs the number of transistors used are less than nor style nand. It drives its name from its construction in which one of the inputs is coupled to its source.

Ain	Bin	Binbar	output
0	0	1	1
0	1	0	1
1	0	1	1
1	1	0	0

Fig 5(b): truth table of source coupled nand gate

As we know that in decoder circuit branching occurs at many points and in this respect this circuit has one special use. Because this circuit can be as fast as an inverter if the branching of source input is large enough or the capacitance seen source input is greater than the output load capacitance for the gate.



**Fig 5(c): output waveforms for source coupled NAND gate**

If source input falls low much before the input at gate and the load capacitance at source is large than at load then it virtually at same speed as that of an inverter. But if gate input arrives before source input then it is proved that if  $(b > 6)$  the circuit works faster than inverter.

### Conclusion:

In this paper, three NAND gate styles are studied and compared to the conventional NAND gate. Of these three, the NOR style NAND and source coupled NAND are shown to have less delay and energy dissipation than the conventional NAND style. These two schemes feature the following comparisons with the conventional NAND.

- The NOR style NAND is 35% faster and 67% more power efficient than conventional NAND design.
- The source coupled NAND style is 36% faster and 82% more power efficient than conventional NAND style.
- Source coupled NAND style is 5% faster and 45% power efficient than NOR style NAND.

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