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Performance Analysis and FPGA Implementation of Digital PID Controller for Speed Control of DC Motor

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Abstract

This paper deals with the performance analysis and implementation of PID(Proportional-Integral-Derivative) Controller on FPGA platform.The hardware implementation has been done on Xilinx Spartan 3E FPGA board.The software implementation has been done using Xilinx ISE 8.1i as a tool and simulation is performed using ModelSim 5.4a as a simulator.The PWM signal is generated by FPGA board,which further given to dc motor for its speed control. A new technique has been introduced for the generation of the control input as a PWM signal for controlling the motor driver circuit and decoding the optical encoder data for using it for the speed feedback in the PID control loop. The VHDL algorithm for the proposed implementation has been presented in this paper. Performance analysis of PID controller using MATLAB software shows the effectiveness of the proposed method.

Keywords: FPGA, Digital PID controller, PWM Generator, Xilinx Spartan 3E, PMDC Motor.

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I. INTRODUCTION

Digital controllers have been widely used over the past five decades due to their simplicity, robustness, effectiveness, and applicability for a broad class of systems. Despite the numerous control design approaches that have appeared in the literature, it is estimated that nowadays digital controllers are still employed in more than 95% of industrial processes. An important feature of these controllers is that they do not require a precise analytical model of the system that is being controlled. For this reason, digital controllers have been widely used in robotics, automation, process control, manufacturing, transportation, and interestingly in real time multi tasking applications.[1].

Implementation of digital controllers has gone through several stages of evolution, from the early mechanical and pneumatic designs to the microprocessor based systems but these systems have the drawback of demanding control requirements of modern power conditioning systems will overload most of the microprocessors and the computing speed limits the use of microprocessor in complex algorithms. Microprocessors, Microcontrollers and Digital Signal Processors (DSPs) can no longer keep pace with the new generation of applications that requires more flexible and higher performance without increasing cost and resources. Furthermore the tasks are executed sequentially which takes longer processing time to accomplish the same task in Microcontrollers and DSPs.We have used Digital PID controller in our work.PID controllers have evolved from analog controllers to digital controllers. The analog controllers are mechanical one and digital controller‟s ranges from microprocessor to SoC platform. The digital domain of control mechanism is less expensive than its analog counterpart; also it is easy to implement the advanced control algorithm. Other advantages of digital domain of control strategies include flexibility in changing parameter, lighter weight and greater insensitivity to noisy external signals[2]. As the growing complexity of motor and motion control applications is increases, it becomes apparent that a reconfigurable hardware such as FPGA offers significant advantage over the microcontroller solutions in the areas of performance, flexibility and inventory control.

Recently, Field Programmable Gate Arrays (FPGA) has becoming alternative solution for the realization of digital control systems. The FPGA based controllers offer advantages such as high speed computation, complex functionality, real time processing capabilities and low power consumption[3]. Hardware Description Languages (HDLs) are used to describe hardware for the purpose of Simulation, Modeling, Testing, Design, and Documentation of digital systems. The most popular HDLs are VHDL [(Very High Speed Integrated Circuit) Hardware Description Language], and Verilog. VHDL is used to describe hardware from the abstract to the concrete level. Many of the Electronic Design Automation (EDA) vendors are standardizing on VHDL as input and output from their tools. These tools include simulation tools, synthesis tools, layout tools and testing tools[4].In the past two years, Spartan II and III FPGA families from Xilinx have been successfully utilized in a variety of applications, which include inverters [5][6], communications [7][8], embedded processors [9], and image processing [10].

II. PWM GENERATOR IMPLEMENTATION

Pulse Width Modulation(PWM) is a technique to provide a logic ”1”and logic “0” for a controlled period of time.Pulse Width Modulation is used in many applications like controlling the speed of a dc motor.A data register is used to store the value for the counter, this value determines the pulse width. The Up/Down counter is loaded with a new value from the data register when the counter reaches its terminal count; a Toggle Flip-flop generates the PWM output.

When the data value is first loaded, the counter begins to count down from the data value to 0. During this phase of operation the terminal count and PWM signals are low. When the counter transitions through zero, the terminal count is generated and triggers the Toggle flip flop to drive the PWM signal high. The data value is reloaded and counting proceeds upto the maximum value. Again a terminal count will be generated when the counter reaches its maximum value, driving the PWM signal to toggle from high to low. The data value is reloaded and the cycle repeats. The direction of the counter is controlled by the PWM signal: the counter is set to count down when the PWM is low and count up when the PWM is high. The terminal count controls the data value that loads to the counter from the data register. Data is loaded when the terminal count is high. The duty cycle of the PWM signal is controlled by the data value loaded to the up/down counter The duty cycle of the PWM output can be varied by specifying various data values, the higher the data value , higher the duty cycle.In this way, PWM Generator has been implemented.

Table 1: Data values for different duty cycles

Data Value	Duty Cycle
11100110	90
11000000	75
10000000	50
01000000	25
00011001	10

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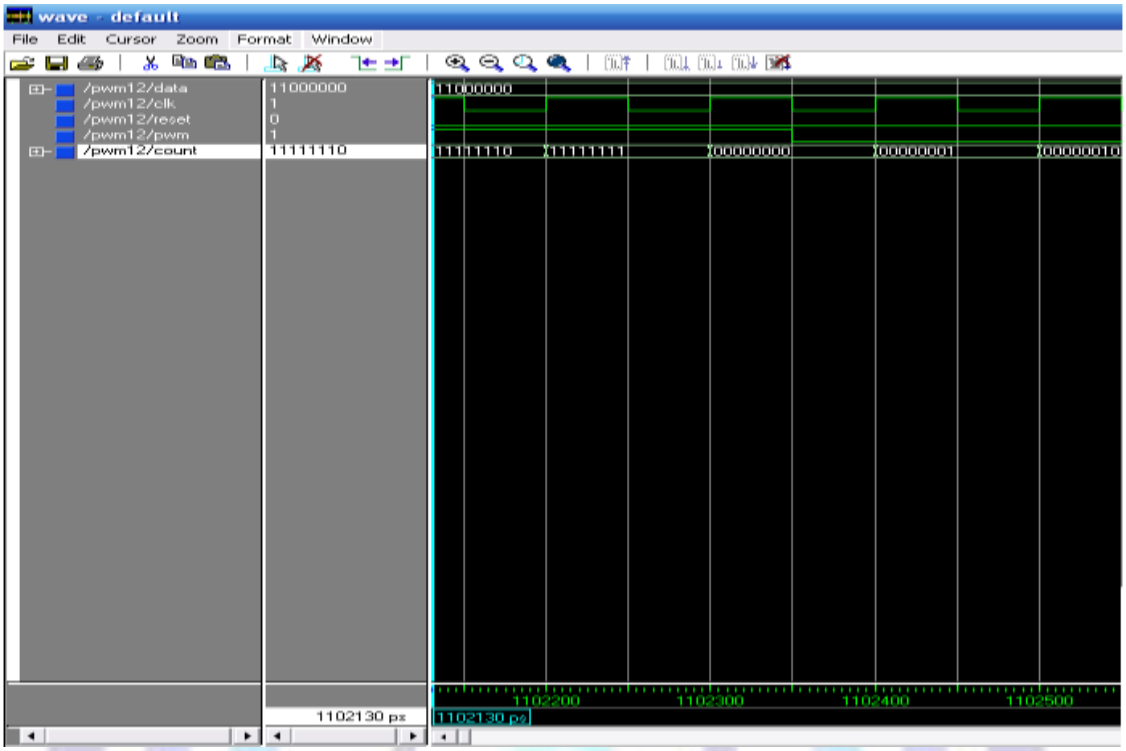

Fig.1 ModelSim Simulator Result for 75% duty cycle

In this way, we have generated PWM signal through ModelSim Simulator.This PWM signal is given as an input to DC motor which helps to drive the motor at different duty cycles..

III. PID CONTROLLER IMPLEMENTATION

Proportional Integral Derivative (PID) controller is the most preferable controller in industries that does not require precise analytical model of the system to be controlled. PID controllers use a 3 basic behavior types or modes: P - proportional, I - integrative and D - derivative. While proportional and integrative modes are also used as single control modes, a derivative mode is rarely used on it' s own in control systems. Combinations such as PI and PD control are very often in practical systems.

The block level diagram of the system is given in Fig.2.PID Controller and PWM generator have been implemented on FPGA platform.The RPM of the motor is sensed by Optical encoder,this encoder produces a signal with the frequency of the signal directly related to the speed of the motor.Now this signal is fed back to the FPGA platform in a closed loop path.By comparing this feedback signal and reference speed signal,an error signal is generated.This error signal works as an input to the Digital PID Controller.The PID Controller then produces the PWM Command signal based on the reference speed and the actual speed of the motor. So system will produce linear output in accordance with the input signal. The PWM system receives a command signal that will be used to produce the desired percent duty cycle for the DC motor[11].

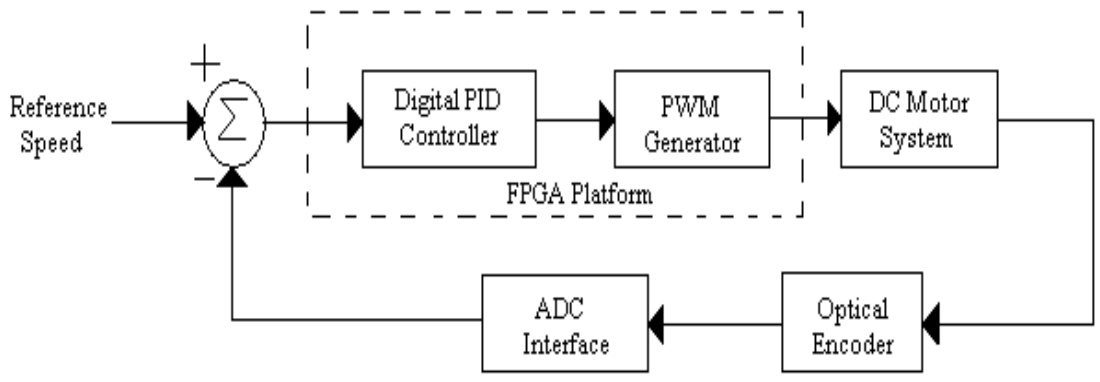

Fig.2 Block level schematic of the system

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The general form of PID controller is given as,

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \quad \text{....(1)}$$

i.e.

$$U(s) = E(s)[K_p + \frac{K_i}{s} + K_d s] \quad \text{....(2)}$$

where, K_p= proportional gain

K_i= integral gain

K_d= derivative gain

Table 2: Motor Parameters Description

Motor Parameters	Value
R_a	1Ω
L_a	0.5 H
J	0.01 kg-m^2
B	0.1 N-m-s
K	0.01 V/rad/s

Table 3: Controller Description

Controller Gains	Value
K_p	100
K_i	200
K_d	10

Before implementing PID controller on FPGA, proper gain values must be selected by observing their step responses on MATLAB tool.After that the selected values are used in VHDL code for PID Controller implementation.The PID Controller has been implemented on Xilinx FPGA using the steps given in [14,15].

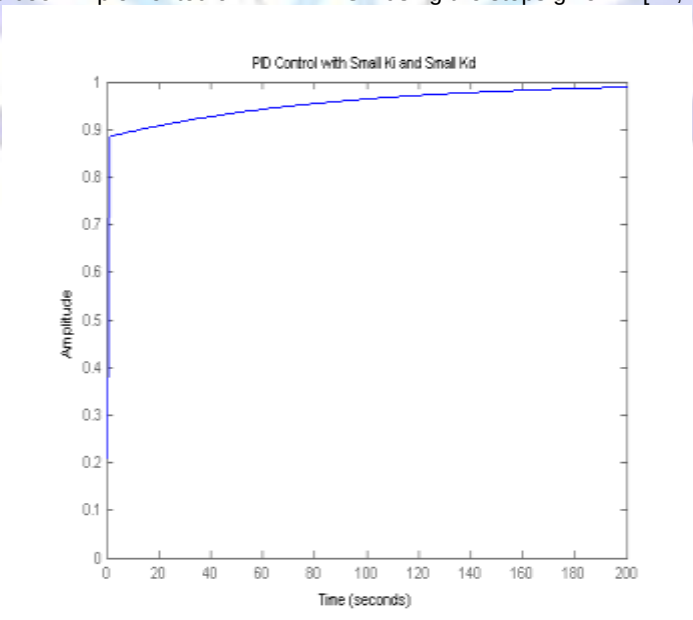

Fig.3 Step response of PID Controller with small Ki and small Kd.

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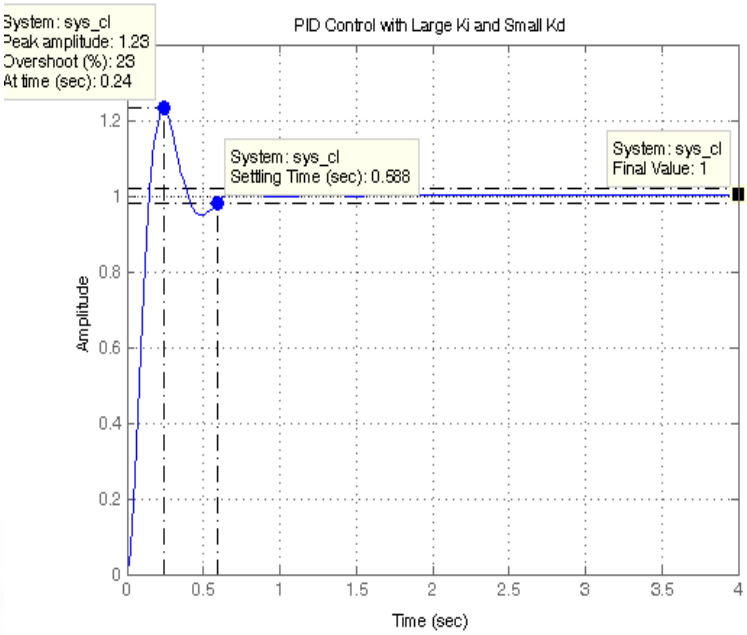

Fig. 4 Step response of PID Controller with large Ki and small Kd.

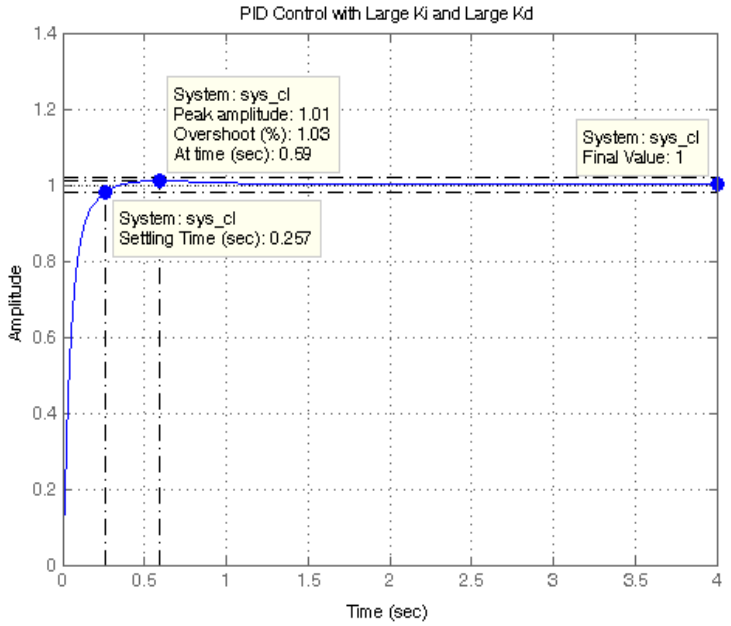

Fig. 5 Step response of PID controller wth large Ki and large Kd.

After seeing all these responses,the response given in fig.5 is the best one to meet the desired specifications.

IV. OPTICAL ENCODER

The DC motor has an optical disc (made by cardboard) mounted on its shaft. The disc has N radial lines on its surface. Consider four slots on the disc (N=4). This will give a resolution of 1/4 in one rotation. An LED (light emitting diode) as transmitter is put at one side of the disc and a photodiode, as receiver is fixed on the other side of the disc. Chip OPT 101 is selected as a photodiode.

Chip LM324 is used as a comparator. When the V_{out} of photodiode is less than V_{ref}, the output of LM324 will be 0V (Low) and when the V_{out} is greater than V_{ref}, the output of LM 324 will be 5V (High). The output signal form LM324 has a frequency which is given by the equation as,

$$f_{out} = \frac{N \, X \, RPM}{60}$$

……(3)

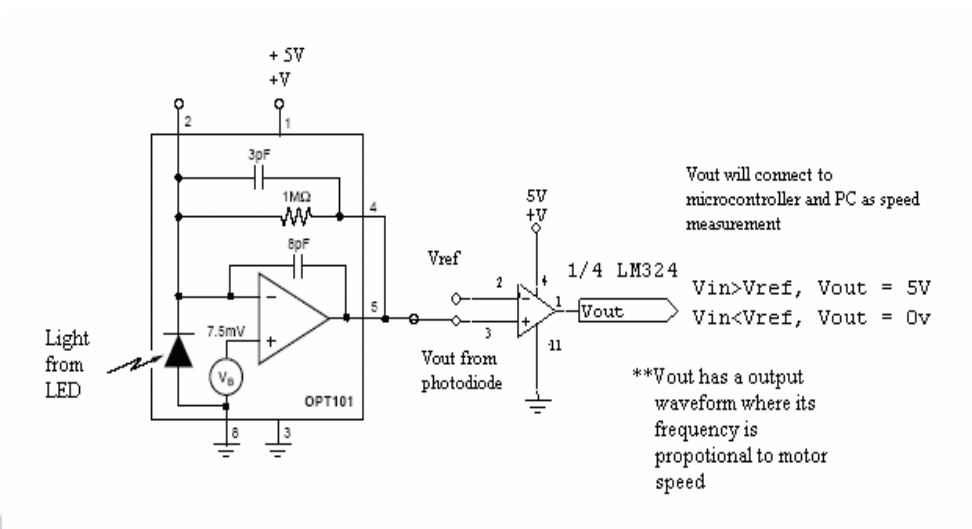

Fig. 6 Optical Encoder Schematic

The Vout pin of the optical encoder is connected to the CRO for observing the frequency waveform which is provided to the PID controller through Analog-to-Digital converter (ADC) interface.

Fig.7 Output waveform of Optical Encoder Circuitry

V. IMPLEMENTATION DETAILS AND EXPERIMENTAL RESULTS

The control algorithm was implemented in a Xilinx Spartan 3E FPGA XC3S250E chip. The average connection delay for the design is 12.006 ns, of which, 66.4% was logic delay and 33.6% was due to route and placing.The maximum frequency of this design is 83.291MHz. The controller,comparator,PWM generator and the encoder interfacing modules have been implemented in the FPGA. The entire system has been implemented using the Xilinx ISE 8.1i as a tool and simulated using ModelSim Simulator 5.4a.

Figure 8 shows the Photograph of the experimental setup and working model of FPGA based DC motor speed control system.

Fig. 8 Experimental setup and working model of FPGA based DC motor speed control system.

VI. CONCLUSIONS

The most promising issue regarding with the FPGAs is the fast time to market operation,speed, accuracy and improvement in cost over other digital implementation techniques. Here speed of PMDC motor is controlled by FPGA platform using PID controller.The design shows significant improvements over the present way of implementing digital controllers in Microcontroller Units in terms of latency, response, flexibility,and robustness. It can be extended to accommodate other advanced digital controllers that may also result into superior, reliable and flexible systems.

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