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# Comparative study of different Sense Amplifiers in 0.18um technology

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## ABSTRACT

A comparative study of different types of sense amplifiers [1] using 0.18um technology is presented. The sense amplifiers under considerations are used in SRAM and DRAM cells.The sensing delay of different types of sense amplifiers are evaluated with respect to variation of bitline capacitance. Comparative results are also provided for the variation in delay with respect to power supply. Extensive results based on 0.18um CMOS technology using CADENCE Spectre simulation tools are presented for different architectures of sense amplifiers. From these results it has been proven that if the output of sense amplifier is isolated from the bitline parasitic capacitance then the sensing delay of sense amplifier reduces.

## Indexing terms/Keywords

Sense amplifier, SRAM, CBL, Alpha latch .

## Academic Discipline And Sub-Disciplines

Electronics and communication ,VLSI design.

## SUBJECT CLASSIFICATION

High speed and low power circuit design, memory design.

## TYPE (METHOD/APPROACH)

All the architectures are simulated and verified on CADENCE tool using 0.18 um technology,level 53 model file. For schematic entry cadence composer is used, for simulation Cadence Spectre 5.1.4 1_ISR.

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## INTRODUCTION

Modern digital systems require the high speed memories for storing and retrieving large amounts of data. Among all memories, SRAM(Static Random Access Memory) is widely used due to its high speed and low power consumption. According to 2002 ITRS [2](International Technology Roadmap for Semiconductors), the 90% area of a chip is occupied by memory by 2013.The various peripheries of SRAM are row decoder, column decoder, control circuitry and Sense amplifier. Among all the peripheral of SRAM,[4] Sense Amplifier is one of the most important peripheral to amplify the small difference between bitlines to full swing. Sense amplifiers are mostly used to read the stored data of SRAM, DRAM [3]cells. The performance of sense amplifiers affects the speed and the power consumption of a memory. Nowadays the size of memory is increasing in a very rapid manner, and hence no. of cells also increases due to which the bitine parasitic capacitance also increases. So with increase in bitline parasitic capacitance the speed of the memory reduces. To overcome this problem we use the high performance sense amplifier. The main function of the sense amplifier is to improve the speed, reduce the power consumption and amplify the small voltage difference of bitlines. Sense amplifiers comprises of a positive feedback circuitry.

## Types of Sense Amplifiers

## Clamped Bitline Sense Amplifier

The clamped bitline sense amplifier is shown in Fig.1. Here M2-M5 act as a high gain positive feedback sense amplifier. M6 and M7 operates in linear region and provides a low impedance clamp between the bitline and ground. M8 and M9 are used to equalize the potential on bitlines. M1 is used to enable the sense amplifier.Sense amplifier operates in two phase precharge phase and sensing phase. In precharge phase EQ signal and EN signalis high so MOS M5 and M6 turns on and forcing the bitlines to same potential and M1 is off. During sensing phase EQ and EN both signals are low so sense amplifiers got enabled and the current diference between the bitlines is sensed by the source terminal of M4 and M5 and corresponding the small difference is amplified by the positive feedback circuitry.The main advantage of clamped bitline sense amplifier is that the output nodes are totally isolated from the bitline capacitance due to which sense amplifier respons very quickly. Also the input nodes of this amplifier are low impedance current sensitive due to which small difference at the bitlines is amplified to the full swing.The drawback of this type sense amplifier is that in this case large no. of MOS devices are required and also extra EQ signal is required to force the same potential at bitlines.

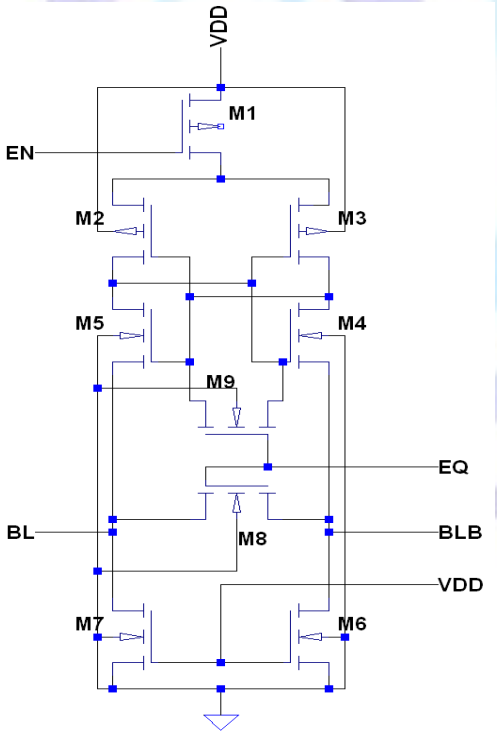


**Fig.1 Clamped Bitline Sense Amplifier [7]**

## Latch Type Sense Amplifier

Latch type sense amplifier is shown in Fig. 2. Here M1-M4 act as high gain positive feedback sense amplifier.M7 and M8 are used to sense the small difference at the bitlines. M5 and M6 are used to precharge the output nodes.M9 is used to enable the sense amplifier.In preharge phase SE signal is low so M5 and M6 turns on and charge the output node. In sensing phase SE signal is high M9 turns on and M7 and M8 act as common source differential amplifier. M1-M4 amplifies the small difference to full swing at output node.Latch Type Sense Amplifier is used due to its high speed and low power consumption and output is also isolated from bitline capacitance. The drawback of Latch Type Sense Amplifier is that the failures caused due to insufficient sensing margin by the input offset voltage.

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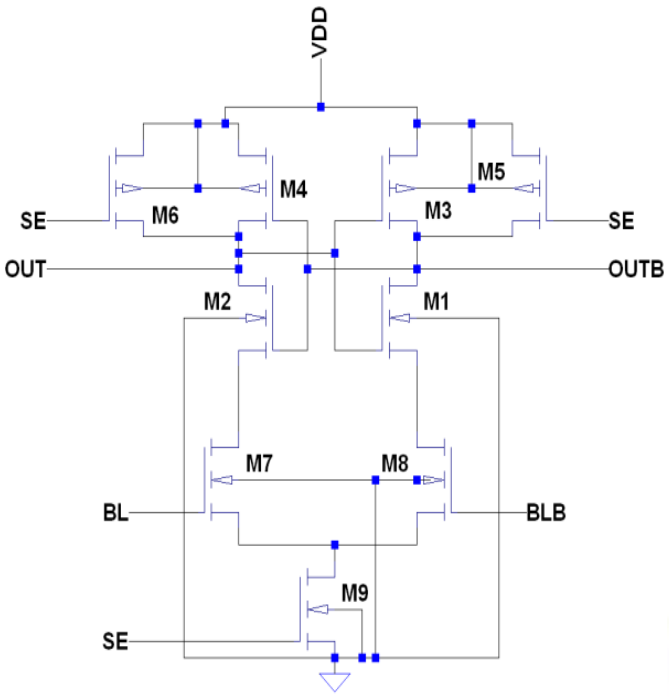


**Fig.2 Latch Type Sense Amplifier [5]**

## Cross Coupled Sense Amplifier

Cross coupled sense amplifier is shown in Fig. 3. Here M1-M4 act as high gain positive feedback sense amplifier. M5 is used to enable the sense amplifier.M8 is used to equalize the output nodes. Here M1 and M2 is biased in Saturation region, M5 is turned on by SAE signal. The small voltage difference at input nodes is amplified by the high gain positive feedback amplifier.The main advantage of this sense amplifier is that less no of MOS transistors are required, so in case of large memory the cost is very less.The main drawback of this type sense amplifier is that in this case output node is not isolated from the bitline parasitic capacitance so due to which with increase in no. of cells the sensing delay of device also increases.

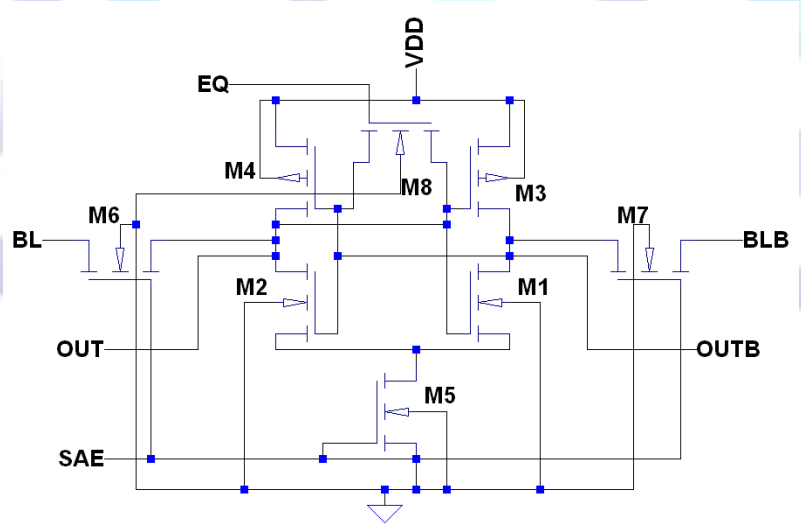


**Fig.3 Cross Coupled Sense Amplifier [6]**

## Hybrid Sense Amplifier

Hybrid sense amplifier is shown in Fig. 4. Here M1,M2,M5,M6 forms the high gain positive feedback amplifier and M9 is used to enable the sense amplifier. M10 is used to equalize the output at same potential. In precharge phase EQ signal is low so M10 turns on and our output nodes are forced at same potential. During sensing phase SE signal is high and the small current difference from the bitlines is sensed by the source terminal of M5 and M6 transistor than positive feedback amplifier amplify the small difference to full swing.The main advantage of this type of sense amplifier is that here output node is totally independent of bitline parasitic capacitance so due to which the sensing delay is quite low or we can say that the speed of operation is high.

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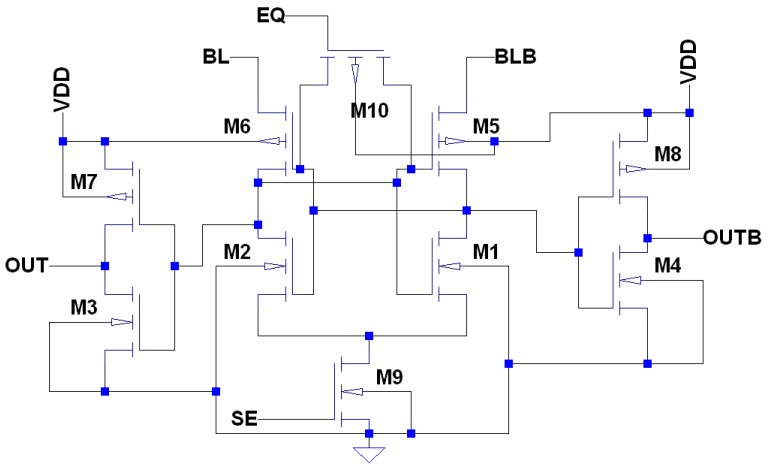
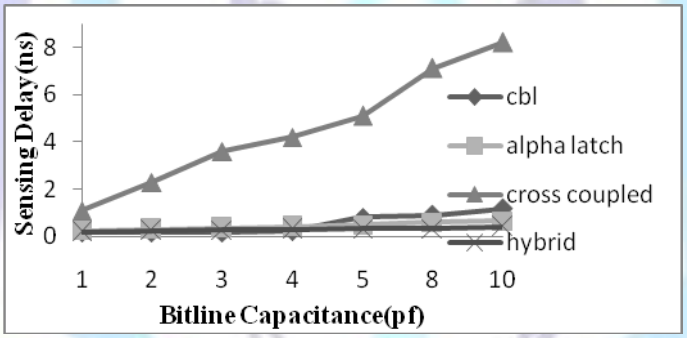



**Fig. 4 Hybrid Sense Amplifier.[9]**

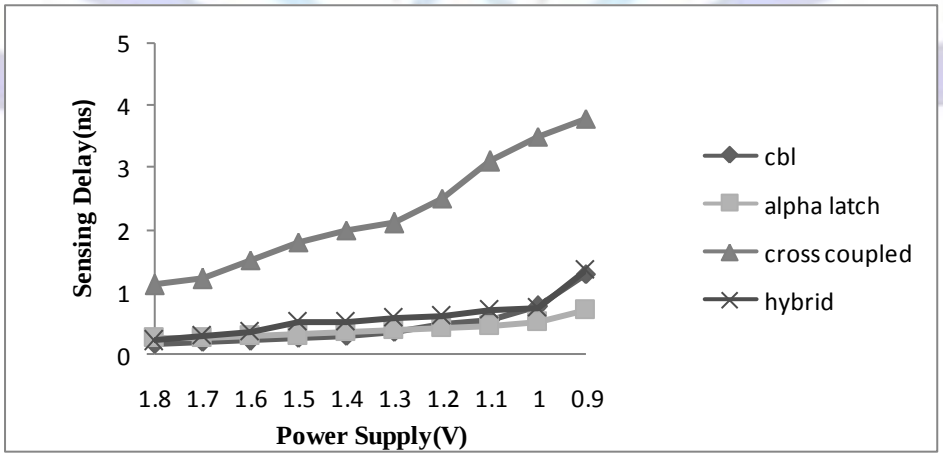
## Simulation Results

The comparision of different sense amplifiers is simulated by using CADENCE tool with spectre simulating tool.The supply voltage used for this work is 1.8V and the channel length is 0.18um.The variation of sensing delay with respect to bitline capacitance is shown in Fig.5 and variation of sensing delay with respect to power supply is shown in Fig. 6 and variation of power dissipation with respect to bitline capacitance is shown in Fig. 7. From these results it is to be proved that power dissipation is increases with increase in bitline capacitance and also the sensing delay insreases with reduction in supply voltage.Also if there is increase in bitline capacitance then the sensing delay of a sense amplifier increases.



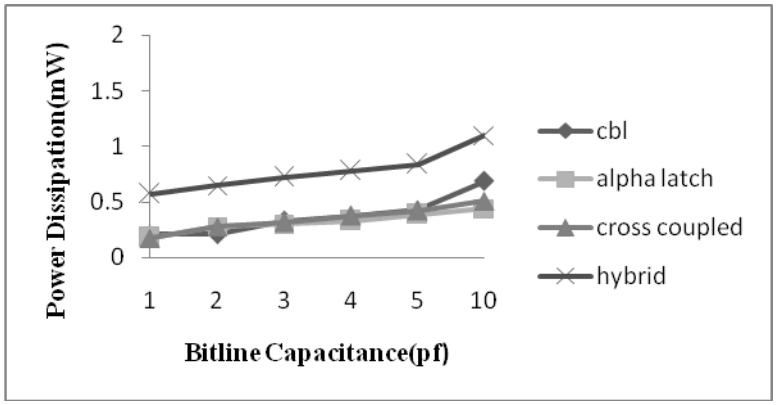

**Channel length = 0.18um, Supply voltage = 1.8 V**

**Fig. 5 Sensing delay of different sense amplifiers with respect to Bitline parasitic Capacitancs**




**Channel length = 0.18um, Supply voltage = 1.8 V, Bitline Capacitance=1pf**

**Fig. 6 Sensing delay with respect to Power supply**




**Channel length = 0.18um, Supply voltage = 1.8 V, Bitline Capacitance=1pf**

**Fig. 7 Power dissipation with respect to Bitline parasitic capacitance**

## Conclusion:

A comparative study of different sense amplifier is carried out using 0.18um CMOS technology. Sense amplifiers are designed using CADENCE tool with SPECTRE simulator. Here simulation results are providing for variation of sensing delay with respect to variation in power supply and bitline parasitic capacitance. Comparing the different architectures of Sense Amplifier Hybrid sense amplifier comprise of minimum delay with variation in bitline parasitic capacitance, but in this case power dissipation is more with variation of bitline parasitic capacitance. Also in case of Alpha Latch sense amplifier and Clamped bitline sense amplifier there is small variation in sensing delay and power with respect to variation in bitline capacitance. Also in case of Cross coupled sense amplifier there is large variation of sensing delay with variation of bitline capacitance so by which the operating speed of this sense amplifier is quite low, but here power dissipation is very less with variation in bitline capacitance. Also the variation of bitline capacitance with respect to power supply is studied so in case of hybrid sense amplifier the variation of dealy is less as compare to other sense amplifiers. According to these results it has been seen that the delay of sense amplifiers is reduced if the output is isolated from the bitline capacitance.

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