



INSTABILITY PROBLEM OF CONVENTIONAL TRANSFORMER DIFFERENTIAL PROTECTION-APPLICATION OF ZERO SEQUENCE CURRENT TRAP

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Abstract

Zero sequence component of current usually causes instability of the differential protection. It enters circuits through earthed terminals. The traditional way of solving the problem in differential schemes is by connecting the interposing current transformers (ICTs) in delta since there is no path for zero sequence component of current in delta. This paper suggests another way of dealing with the problem. A zero sequence trap is modeled to pass the zero sequence current through an output logic which ensures that operation of the relay is enabled only when there is a real differential fault.

Key words: differential current, zero sequence component of current, differential protection, output logic, instability, ferroresonance



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INTRODUCTION

The conventional differential protection suffers from instability due to:- (i) tap changer error (ii) transformer switching magnetizing in-rush current (iii) emergence of zero sequence component of current, etc. These problems are solved in different ways.

1.1 Tap changer error

Since in transformer, $n_1/n_2 = I_2/I_1 = V_1/V_2$, any change in the number of turns will cause a change in the current and voltage. So in order to keep the differential relay stable, the tap changer error must be accommodated in relay setting. $E_t = E_1 + E_2 + \dots + E_n$. Where E_t is the total accommodated error, E_1, E_2 , etc, are other errors. Care must be taken in determining the magnitude of E_t so that the sensitivity of the relay is not impaired.

1.2 Switching inrush current of transformer

When a transformer is switched on, the vibrations in the lamination produce high transient current on the switched side. See fig A1, in the appendix. However this dies down after few milliseconds. Since the currents on both sides of the differential relay are not equal during the switching transient, the relay operates. The traditional way of solving this problem is by installing harmonic filter in the relay to block the harmonic signals. The author has modeled a new approach to this problem. See [10S].

1. EMERGENCE OF ZERO SEQUENCE COMPONENT OF CURRENT

Zero sequence component of current always finds its way into circuits through earthed terminals and offsets

the stability of the differential protection. The traditional way of solving this problem is by connecting the current transformers (or interposing current transformers) in delta, since there is no path for zero sequence current in delta.

In this paper a zero sequence trap is modeled to block the zero sequence component of current from offsetting the stability of the differential protection scheme.

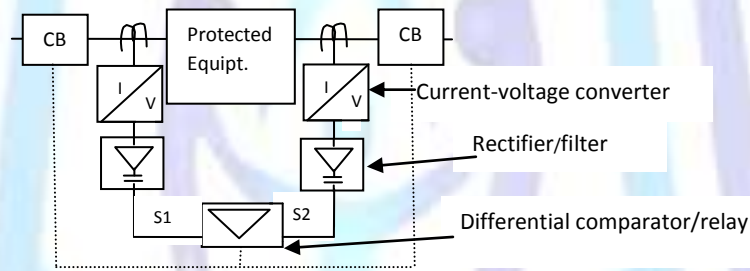


Fig.1: The basic 2 -input differential protection scheme

PRINCIPLES OF OPERATION

Let the inputs to the differential protection be S1 and S2 such that

$$\left. \begin{aligned} S_1 &= K_{11} I_1 Z_1 \\ S_2 &= K_{21} I_2 Z_2 \end{aligned} \right\} (1)$$

Where $I Z$ = current converted to voltage

$K_{11}; K_{21}$ = Conversion factors.

$$\text{For stability, } |K_{11} I_1 Z_1| = |K_{21} I_2 Z_2| \quad (2)$$

If $K_{11} = K_{21} = K$ and $I_1 = I_2 = I$, equation (2) now becomes

$$|K I Z_1| = |K I Z_2| \quad (3)$$

Thus for stability Z_1 must be equal to Z_2 . Otherwise that is a condition of an uneven lengths of the current transformer (CT) pilots or/and unequal rated burdens of the input current transformers (CTs). Depending on the magnitude of $|Z_1 - Z_2|$, it could cause the differential current, I_Δ , to rise above the tolerance limit. Therefore in order to guarantee stability, means for compensation for difference impedance, Z_Δ , must be provided.

In eqn(3), let $Z_1 = K_3 R_1$ and $Z_2 = K_4 R_2$ Then;

$$|K K_3 I_1 Z_1| = |K K_4 I_2 Z_2| \quad (4)$$



Where K3 and K4 are conversion factors..

Applying the signals of eq(4) into two different amplifiers with reference signals Sr1 and Sr2(in the processor) the output expression becomes:

$$A_1(I_1 K_3 R_1 - S_{r1}) = A_2(I_2 K_4 R_2 - S_{r2})$$

where A1 and A2 are the amplifiers' gains.

Therefore $|A_1(KK_3 I_1 R_1 - S_{r1})| = |A_2(KK_4 I_2 R_2 - S_{r2})|$ (5)

If A1 = A2 = A; and K3 = K4 (Similar Circuits), then eqn (5) becomes

$$|x(I_1 R_1 - S_{r1})| = |x(I_2 R_2 - S_{r2})| \quad (6)$$

where x = AK K3 = A K K4

x1R1-Sr1 and xI2R2-Sr2 are suppose to be equal but where they are not, they can be made equal by simply adjusting Sr1 or Sr2 .

The ports $|x(I_1 R_1 - S_{r1})|$ and $|x(I_2 R_2 - S_{r2})|$ are the complementary out-puts of the differential circuit; while Sr1 and Sr2 are can be called the "restraining signals".

By feeding the signals of equation (6) into a window comparator with gains B1 and B2, the final outputs of the differential circuit become;

$$\left. \begin{aligned} &|B_1 x(I_1 R_1 - S_{r1})| \quad |B_2 x(I_2 R_2 - S_{r2})| \\ \text{and} \quad &|B_2 x(I_2 R_2 - S_{r2})| \quad |x(I_1 R_1 - S_{r1})| \end{aligned} \right\} (7)$$

Again Since the circuits are identical

$$B_1 = B_2 = B, S_{r1} = S_{r2} \text{ and } R_1 = R_2 = R$$

Hence eqn (7) can be reduced to:

$$\left. \begin{aligned} &B[m(I_1 - I_2)] \\ &B[m(I_2 - I_1)] \end{aligned} \right\} (8)$$

where m = xR.

Eqn (8) can still be written as

$$\left. \begin{aligned} &C(I_1 - I_2) \\ &C(I_2 - I_1) \end{aligned} \right\} (9)$$

Where C = Bm

Equation (9) shows that the output of the modeled differential circuit is dependent on the differential current, IΔ, although the circuit works on voltage.

When I1 = I2, the output is zero, signifying the stability condition for the differential circuit and I1 ≠ I2 produces two complementary signals of the same magnitude but opposite polarities at the two output terminals of the processor. These output voltages are proportional to the differential current, IΔ.

I1 ≠ I2 can be caused by a real fault or a non-real fault such as in the condition of emergence of zero sequence current. Unless the zero sequence component of current, Iz, is taken care of, the differential protection will remain unstable.

When Iz is present, eqn(9) is modified to

$$\left. \begin{aligned} &C[(I_1 + I_z) - I_2] \\ &C[I_2 - (I_1 + I_z)] \end{aligned} \right\} (10)$$

And this cannot be zero, So the stability of the relay is offset.

In order to block the zero sequence current, the relay output must be governed by the following boolean equation:

$$(I_{\Delta} + \bar{I}_z) \cdot (I_{\Delta} + I_z) = Y \quad (11)$$

One way of implementing eqn (11) is shown in fig 2

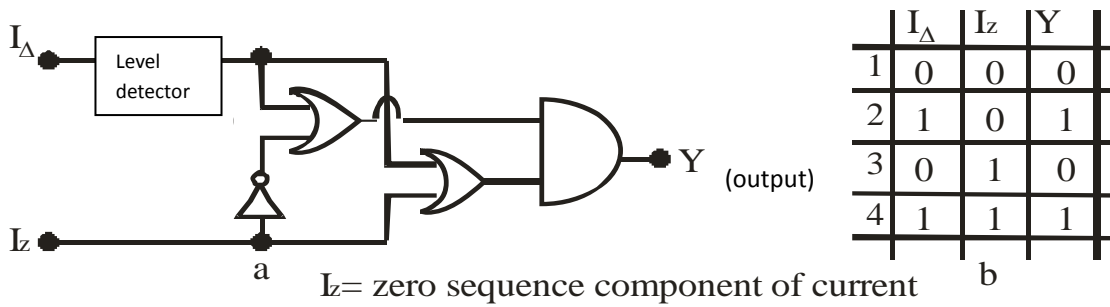


Fig 3.4: Zero Sequence current Trap and truth table

Fig. 2: The relay output logic and the truth table

The output logic ensures that the operation is enabled only when there is a real differential current, I_{Δ} . It can be seen also from the accompanying truth table, that there is output only when there is differential current (conditions 2 and 4).

3.1 DERIVATION OF THE SIGNAL I_z

The signal I_z , is generated at the zero sequence current trap shown in fig. 3.

The 10A MCB has one normally closed contact and one normally opened contact.

The MCB is usually in closed position so that at the emergence of zero sequence current, I_z flows from earth, through R_z and triggers the thyristor, Th, to charge the I_z bus at the output logic. If I_z is more than 10A, the MCB trips and energizes relay, C, which closes its contact to send an alarm to the attendant, at the same time charge the I_z bus at the output logic.

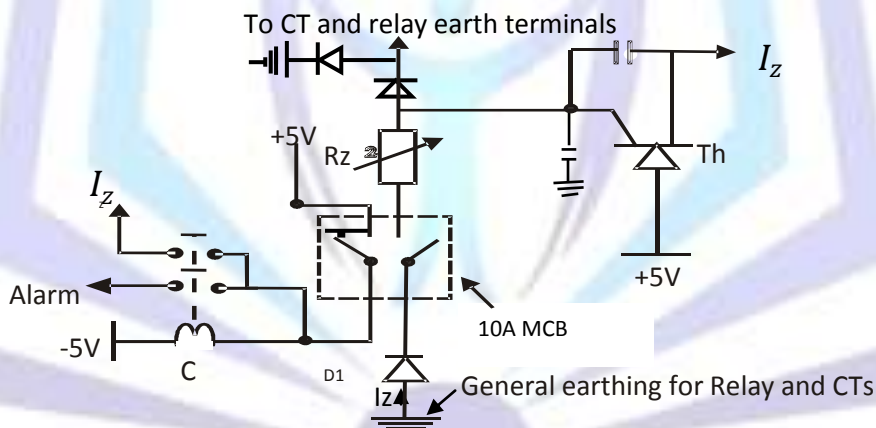


Fig3. Generation of the signal I_z from zero sequence current trap

The conditions for the trap to work effectively are that:

The earthing for all the differential CTs and the relay must be common as shown in fig3.

Appropriate size of conductors must be used for earth leads in order to carry large amount of current.

TESTS AND SIMULATIONS

The simulation results of zero sequence current trap and its logic are shown in figs. 4, 5, 6, 7 and 8. The output of the differential relay was zero when both I_z and I_{Δ} were zero. The conditions when the relay had outputs were seen at $I_z=0V$, $I_{\Delta}=5V$ and at $I_z=5V$, $I_{\Delta}=5V$ (Figs 5 and 6). These simulation results show that the differential relay operates only when there is differential current. Therefore emergence of zero sequence component of current cannot offset the stability of the relay

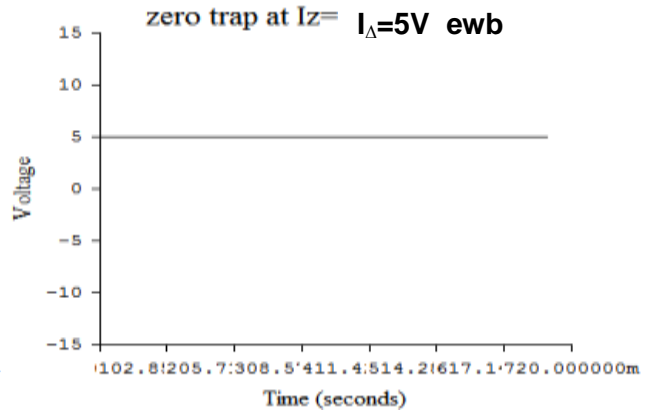
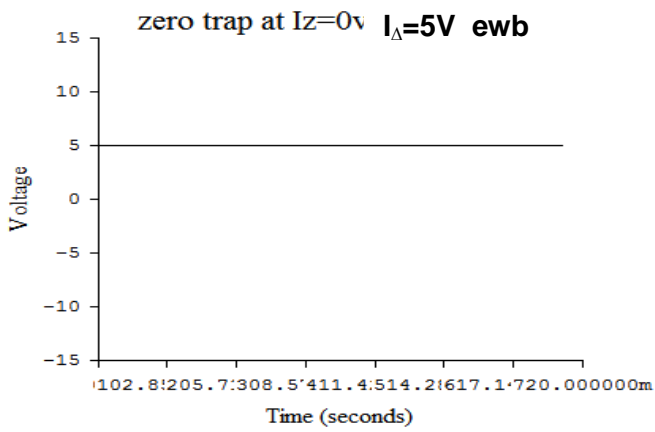
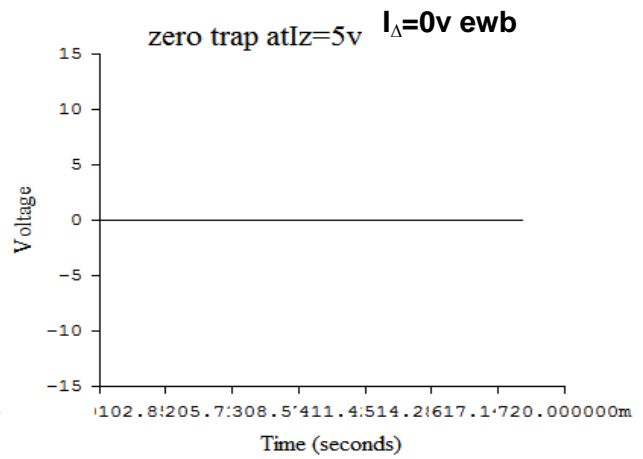
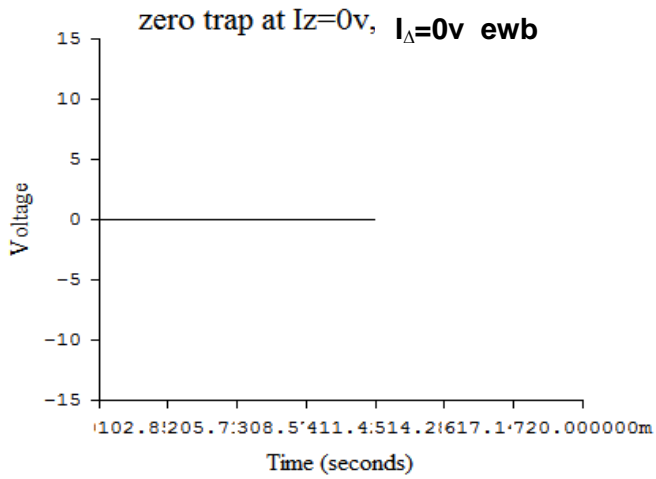
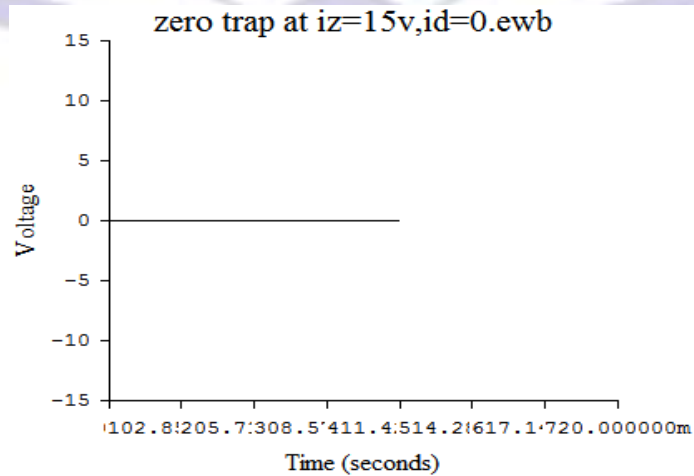


Fig8: relay output when $I_z=15V$ and $I_\Delta=0V$



5. CONCLUSION

The differential protection relay capable of remaining stable under the emergence of zero sequence component of current is presented. The simulation results show that the relay can operate only when there is real differential fault. It remains stable when there is no differential fault irrespective of the magnitude of the zero sequence component of current. This model of differential protection does not require interposing current transformers connected in delta to block the zero sequence component of current from offsetting the differential protection relay.

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APPENDIX

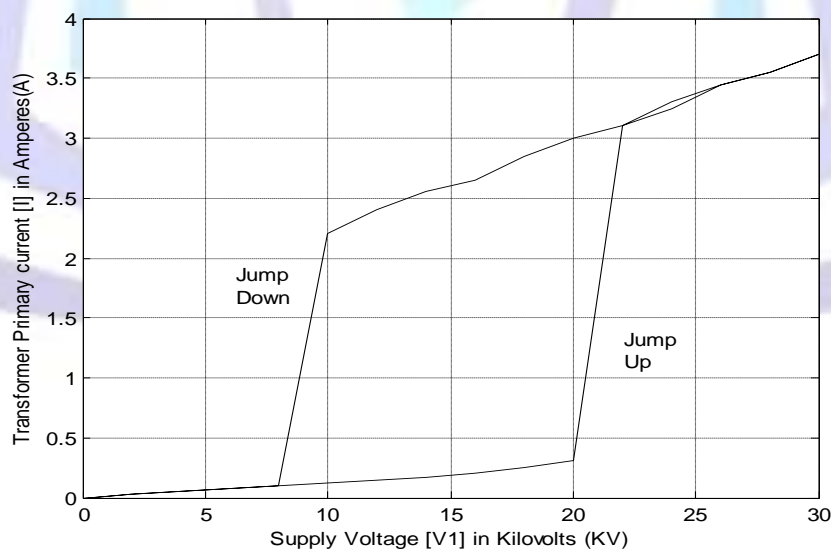


Fig A1: The nature of the switching in-rush magnetizing current when a transformer is switched on.

When the transformer was switched on, the primary current rose linearly from 0 to about 0.3Amps and suddenly jumped to 3Amps. On collapsing, it took another path back to zero. This presents a figure that looks like the hysteresis loop.