

DESIGN OF CMOS LOW DROP-OUT REGULATORS: A COMPARATIVE STUDY

Ashvani Kumar Mishra, Rishikesh Pandey
Thapar University, Patiala, India

Email ID: ashvani.mishra@gmail.com, riship23@gmail.com

ABSTRACT

The advancement in battery operated portable devices, noise sensitive devices and other devices, which need high precision supply voltages has fuelled the growth of Low Drop-Out Regulators. Low Drop-Out Regulators showed advantage over its counterpart. The design of Low Drop-Out Regulators with high performance and less Die area is challenging problem now-a-days. This paper is a study of various techniques that are used to achieve better performance of low drop-out regulators.

KEYWORDS

Compensation techniques, Integrated circuit, Low Drop-Out Regulator, Low-voltage.

1. INTRODUCTION

Supplying and conditioning power are the most elementary functions of an electrical system. Any loading application, such as a pager, cellular phone and bio-medical devices can not sustain itself without energy, and can not fully perform its functions without a stable supply. The fact is transformers, generators, batteries, and other off-line supplies get substantial voltage and current variations across time and over a wide range of operating conditions. They are normally jittery and noisy not only because of their inherent nature but also because high-power switching circuits like digital signal-processing circuits (DSP) and central-processing units (CPUs) usually load these devices. The rapidly changing loads cause transient excursions in the supposedly noise-free supply, the end results of which are undesired voltage drops and frequency boosts where only a dc component should exist [1]. Use of switching power supply or DC to DC converter, provides portable applications to operate in noisy environments. Mostly electronic systems are very sensitive to noise present on power supplies. Consequently, they require large battery filters to reduce the ripple on battery voltage [2]. The explosive proliferation of battery-powered equipment in the past decade has accelerated the development and use of Low Drop-out voltage regulators for noise sensitive circuits [2, 3]. Low drop-out regulators is driven by the growing demand for higher performance power supply circuits [4]. The low drop-out nature of the regulator makes it suitable for use in many applications, namely, automotive, portable and biomedical applications. The automotive industry requires low drop-out regulators to power up digital circuits, especially during cold-crank conditions where the battery voltage can be below 6 V. The increasing demand, however, is especially appear in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops. In a cellular phone, for instance, switching regulators are used to boost up the voltage but LDO's are cascaded in series to suppress the inherent noise associated with switching regulators. LDO's benefit from working with low input voltages because power consumption is minimized accordingly, $P = I_{Load} * V_{in}$. Low voltage and low quiescent current are intrinsic circuit characteristics for increased battery efficiency and longevity. Low voltage operation is also a consequence of process technology. This is because isolation barriers reduce as the component densities per unit area increase, thereby exhibiting lower breakdown voltages. Therefore, low power and finer lithography require regulators to operate at low voltages, produce precise output voltages, and have characteristically lower quiescent current flow [5]. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while minimizing quiescent current flow to increase battery life. Current efficiency is particularly important because at low load-current conditions the life of battery is adversely affected by low current efficiency in other words, high quiescent current flow [6]. In this paper, different techniques to improve the performance parameters of low drop-out regulators will be covered. The organization of this paper is as follows: Section 2 will introduce the LDO block description and specifications. Section 3 will cover the structures of LDO with capacitors and discussion of special topology used in designing the LDO. Section 4 will discuss the LDO topologies with external capacitor free architecture. Experimental results will be included in Section 5. Finally in section 6 conclusion of this paper will be discussed.

2. LOW DROP-OUT REGULATOR BLOCK DESCRIPTION AND SPECIFICATIONS

Low Drop-out Regulators as shown in Fig. 1 are composed of four basic components: a voltage reference, an error amplifier, a pass element, and a feedback network.

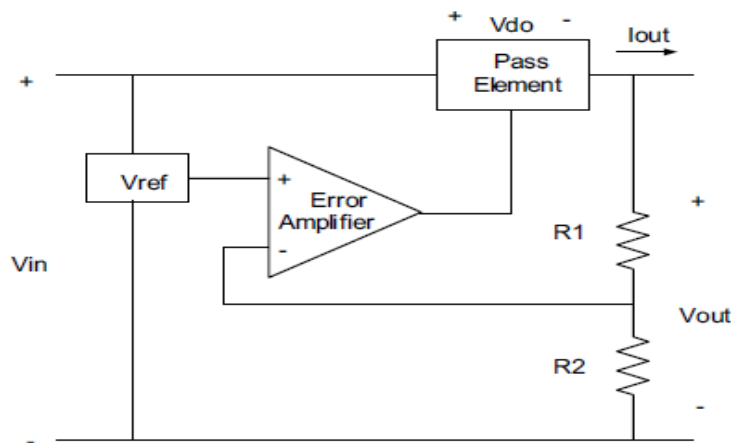


Fig. 1 Basic Low Drop-out Regulator Block Diagram [7].

The Voltage Reference provides a precise output voltage for the operation of the regulator. Voltage references, unlike regulators, have a poor load driving capability.

The Error Amplifier produces an error signal whenever the sensed feedback output differs from the reference voltage. The error output is used to control the amount of current the pass element allows into the load. The resulting control seeks to set the value of output voltage (V_{out}) to a level where the error signal is as close as possible to zero.

The Pass Element provides the output current needed to drive the load, under the control of the error amplifier. Several configurations of the pass element have been proposed, depending on the system specification. The most widely used configurations include NMOS transistor and common source PMOS transistor. PMOS transistors are typically the best overall choice yielding a good compromise of dropout voltage, quiescent current flow, output current, and speed. The circuit design of an LDO is thoroughly affected by the physical requirements of the pass element. The pass element must be physically large to yield high output currents and low dropout voltage characteristics.

The Feedback Network produces the output voltage to be compared with the voltage reference. This voltage is produced by a voltage divider described by the equation 1.

$$V_{out} = V_{ref} \left(1 + \frac{R_1}{R_2} \right) \quad (1)$$

Feedback network can be designed using passive elements (resistors) or active elements (transistors) [7].

Three categories describe the operating performance of a linear regulator: (1) dc- and ac-regulating (accuracy) performance, (2) power characteristics, and (3) operating requirements [3, 8].

3. LOW DROP-OUT REGULATORS

Low drop-out regulators provide constant supply rail suitable for power management. On the basis of stability and chip area, LDO are of two types namely Low Drop-Out Regulators with Capacitor and Low Drop-out Regulators without capacitor. Capacitor free LDO utilises external capacitor for stability on the cost of chip area. Chip area problem can be solved by using on-chip LDO, which utilises the different compensation techniques for stability without using external capacitor. Detail discussion on LDOs with capacitor and capacitor free LDOs are discussed in sections 3.1 and 3.2 respectively.

3.1 Low drop-out regulators with capacitor

The several authors have been reported low drop-out regulators with capacitor [9-14]. Leung *et al.* [9] proposed a low drop-out structure to reduce board space. The structure utilises damping-factor control frequency compensation scheme along with first-order high-pass feedback network. Due to virtue of this scheme, this structure provides high stability, load transient and fast line load transient responses. Adaptive miller compensation (AMC) technique based LDO structure in [10] provides high stability, as well as fast line and load transient responses. This structure also provides good performance on PSRR at high frequency. However, there are some disadvantages with this structure. The gain-band width (GBW) of this LDO is directly proportional to trans-conductance of pass device, which depends on output current, so it is not suitable for large current design. Oh *et al.* [11] presented an LDO with current feedback amplifiers (CFAs) as shown in Fig. 2. The suggested LDO provides fast response and high slew rate with class-AB operation.

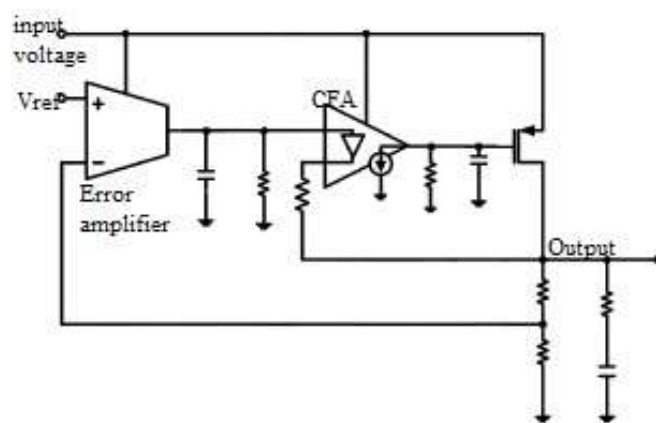


Fig. 2 LDO structure using CFA based buffer amplifier [11].

CMOS LDO has measure problem of high impedance feedback path which has been solved in the suggested structure. This structure utilizes a low ac impedance feedback path to achieve fast response while maintaining low quiescent power consumption. The low ac impedance feedback path is constructed using a CFA based second-stage buffer. CFAs are popular to provide fast response with minimum slew-rate limiting. It uses global voltage mode feedback for steady state accuracy. The LDO structure with an impedance attenuated buffer for driving the pass device has been suggested in [12]. In the structure error amplifier has been realised by single-stage folded-cascode structure. This LDO structure is stabilized by using current-buffer (or cascode-Miller) frequency compensation, which is a pole-splitting compensation designed for splitting of two poles. The use of the current-buffer compensation scheme allows the amplifier to achieve wider unity-gain frequency, improved stability and enhance PSRR. Man *et al.* [13] presented a LDO structure using flipped voltage follower (FVF) cell. By using FVF in the structure, the output impedance is reduced which provides better stability than conventional LDO. The loop bandwidth at low load current is independent of the load current. It has wider bandwidth than the conventional LDO. The LDO structure based on CFA with inverting output buffer suggested in [14] is shown in Fig. 3. Very low impedance at the inverting input of the CFA is the reason to achieve high regulation and fast transient response of this structure. The use of CFA in the circuit gives excellent performance in terms of bandwidth and slew rate.

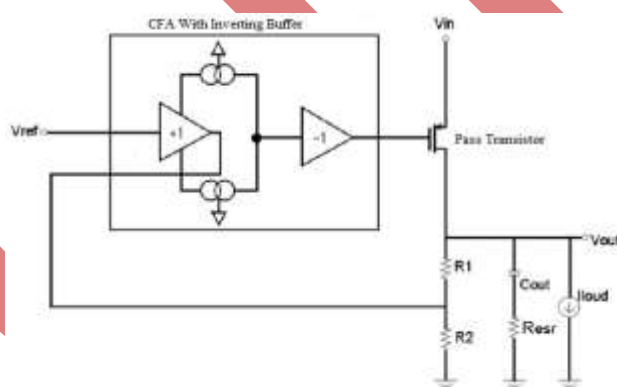


Fig. 3 LDO Architecture Based On CFA With Inverting Output Buffer [14].

3.2. Capacitor free low drop-out regulators

Capacitor free low drop-out regulators have several advantages over the low drop-out regulators with capacitance discussed in section 3.1 on the basis of small size and portability. Hazucha *et al.* [15] proposed a LDO structure, which uses replica-biased source follower for multi-supply voltage. This topology achieves very fast response time and good figure of merit which accounts for the decoupling capacitance, output drop, current efficiency and current rating. The LDO structure with a capacitor-multiplier frequency compensation technique suggested in [16] is shown in Fig. 4. This technique eliminates the cascode structure or buffer stage, due to which suggested LDO facilitates low voltage operation.

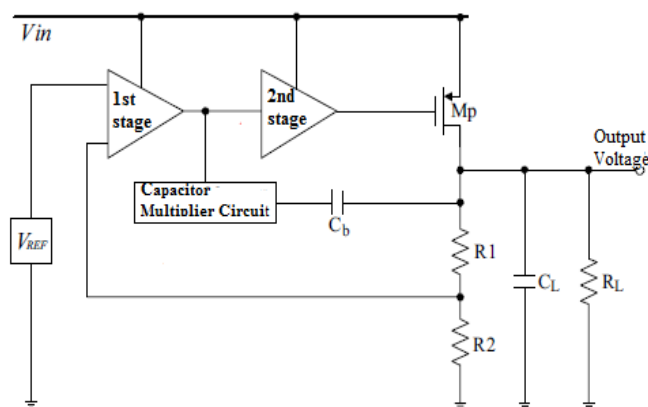


Fig. 4 LDO with Capacitor-Multiplier Frequency Compensation [16].

Shiyang *et al.* [17] has been presented a LDO using Damping-factor-control (DFC) block along with miller compensation shown in Fig. 5.

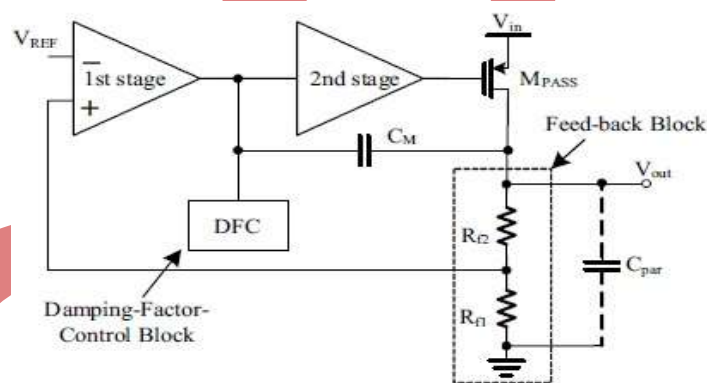


Fig. 5 Structure of LDO with DFC Block [17]

By using Miller compensation, a low frequency dominant pole is internally generated, and two other non-dominant poles, which frequency are higher than unity gain frequency (UGF), which is configured by DFC block. DFC block is placed in between first and second stage. Stability has been achieved by Miller and DFC compensation, through the opposed zero cancellation. A capacitor less LDO structure with an input current differencing technique to achieve sleep-mode efficiency and area saving is proposed in [18]. Instead of using an operational amplifier as the error amplification block, it consists of a current differencing (CD) stage. There were two main advantages when the techniques were implemented in an LDO. Firstly, it allows low voltage operation. Secondly, this configuration renders a smaller feedback factor that helps reducing the excessive loop gain that threatens stability in zero loads. Kamal *et al.* [19] proposed a topology which does not require an external capacitor for their stability. They use PMOS as pass device and implement a compensation circuitry in between output of error amplifier and drain of pass devices for improving its performance over uncompensated system. A LDO with NMOS as a pass device proposed in [20] consists of an error amplifier, a floating voltage source, the pass element, and the feedback network. This architecture uses switched floating capacitors to take advantage of using NMOS transistor as a pass device. Wang *et al.* [21] have suggested high precision low dropout regulator with nested feedback loops. A zero-tracking compensation loop is nested inside of the negative feedback loop comprising an error amplifier. It utilises PMOS transistor as pass device. This structure is independent of off-chip capacitor and effective series resistance (ESR).

4. COMPARISON

Low drop-out regulators with capacitor and without capacitor low drop-out regulator are discussed in sections 3.1 & 3.2 and their simulated results are tabulated in Tables 1 & 2, respectively. From Table 1, it can be seen that the LDO suggested in [14] has higher regulation, current efficiency and PSRR than the existing LDOs. It can also be observed that low drop-out regulators with capacitor occupy large area due to the use of load capacitor for stability.

Table (1) Comparison of Different Low Drop-out Regulators with capacitor

Parameters	Unit	[9]	[11]	[12]	[13]	[14]
Year	-	2003	2007	2007	2008	2012
CMOS Process	μm	0.6	0.25	0.35	0.35	0.35
Drop-out Voltage	mV	200	—	54	—	99.8
C_L	μF	10	0.05	1	1	1
ESR	ohm	1	0.1	N.A.	0.016	-
Ground Current(I_q)	mA	-	0.1	0.02	6	59-189
PSRR	dB	-60 at 10Hz	>43 at 30kHz	—	—	>56 at (0 Hz-100 MHz)
Current Efficiency	%	—	99.8	99.8	-	99.8
Line Regulation	mV/V	—	—	2	18	13.5
Load Regulation	mV/mA	—	—	0.17	0.28	0.025
Area	mm^2	0.31	0.23	0.264	4.48	—

Table (2) Comparison of Different Low Drop-out Regulators without Capacitor

Parameters	Unit	[15]	[16]	[17]	[21]
Year		2005	2008	2009	2011
CMOS Process	μm	0.09	0.18	0.25	0.35
Drop-out Voltage	mV	90	160	50	110
C_L	μF	-	-	-	-
ESR	ohm	-	-	-	-
Ground Current (I_q)	mA	6	0.2	0.04	0.05
PSRR	dB	-	70 at 10k Hz	-80 at 1kHz	>50 at 3kHz
Current Efficiency	%	94.3	99.99	-	-
Line Regulation	mV/V	-	1.27%	-	0.012%
Load Regulation	mV/ mA	-	0.002%	-	0.005%
Area	mm^2	0.008	-	-	0.756

From table 2, it can be seen that LDO suggested in [21] has higher PSRR and regulation than the existing LDOs. Due to the use of special compensation schemes and topologies high regulation, current efficiency and PSRR is achieved without using external capacitor. Also these structures occupy less chip area with desired performance specifications such as current efficiency, regulation and PSRR.

5. CONCLUSION

A Low Drop-Out Regulator is capable of keeping its specified output voltage over a wide range of load current and input voltage. LDO provide constant supply rail for integrated circuits. Many of the LDOs in today's portable devices are integrated into multifunction Power-management integrated circuits. Stability is major concern for LDO design, which can be achieved by either using external capacitor or by using some special compensation techniques with improved topologies. There is limit on on-chip capacitor value so for stability off-chip capacitance in combination with effective series resistance is used. But for portable applications there are many LDOs which utilize on-chip capacitor with different specific schemes for compensation. In this paper, LDO design techniques and different topologies to improve its stability and performance have been discussed.

REFERENCES

- [1] G. A. Rincon-Mora. 2009. Analog IC design with low-dropout regulators. McGraw Hill New York.
- [2] Armani and H. Cordonnier. 2004. Power and battery management ICs for low-cost portable electronics. in Annales Telecommunications, vol.59, no. 7-8, pp. 974-983.
- [3] C. Simpson. 1997. A User's Guide to Compensating Low-Dropout Regulators. In Proceeding of IEEE Santa Clara conference, CA, pp. 270-275.
- [4] G. A. R.-Mora and P. E. Allen. 1998. Optimized Frequency-Shaping Circuit Topologies for LDO's. IEEE Transactions on Circuits and Systems—ii: Analog and Digital Signal Processing, vol. 45, No. 6, pp.703-707.

- [5] G. A. Rincon-Mora and P. E. Allen. 1988. A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator. IEEE Journal of Solid-State Circuits, Vol. 33, no. 1, pp. 36-43.
- [6] G. A. Rincon-Mora. 1996. Current efficient, low voltage, low drop-out regulators. Ph.D. dissertation, Elect. Comp. Eng. Dept., Georgia Inst. of Technology, Atlanta.
- [7] P. M. A.-Morales, C. J. O.-Villanueva, R. Perez, R.P.-Garcia and M. Jimenez. 2004. Design of an Adjustable, Low Voltage, Low Dropout Regulator. In Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, Dominican Republic, pp.289-292.
- [8] C. K. Chava and J. Silva-Martinez. 2004. A Frequency Compensation Scheme for LDO Voltage Regulators. IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 51, no. 6, pp. 1041-1050.
- [9] K. N. Leung and P. K. T. Mok. 2003. A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation. IEEE Journal of Solid State Circuits, vol. 38, no. 10, pp. 1691–1702.
- [10] X. Lai, J. Guo, Z. Sun and J. Xie. 2006. A 3-A CMOS low-dropout regulator with adaptive Miller compensation. Analog Integr Circ Sig Process, vol. 49, pp. 5-10.
- [11] W. Oh and B. Bakkaloglu. 2007. A CMOS Low-Dropout Regulator with Current-Mode Feedback Buffer Amplifier. IEEE Transactions on Circuits and Systems—II: Express Briefs, vol. 54, no. 10, pp. 922-926.
- [12] M. Al-Shyoukh, H. Lee and R. Perez. 2007. A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation. IEEE Journal of Solid-State Circuits, vol. 42, no. 8, pp. 1732-1742.
- [13] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok and M. Chan. 2008. Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC. IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 55, no. 5, pp. 1392-1401.
- [14] A. Saberhari, E. Alarco and S. B. Shokouhi. 2013. Fast transient current-steering CMOS LDO regulator based on current feedback amplifier,” Integration, the VLSI Journal, vol. 46, no. 2, pp. 165-171.
- [15] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan and S. Borkar. 2005. Area-Efficient Linear Regulator with Ultra-Fast Load Regulation. IEEE Journal of Solid-State Circuits, vol. 40, no. 4, pp. 933-940.
- [16] Z. Yan, L. Shen, Y. Zhao and S. Yue. 2008. A Low-Voltage CMOS Low-Dropout Regulator with Novel Capacitor-Multiplier Frequency Compensation. IEEE International symposium on Circuits and Systems in Beijing, pp. 2685-2688.
- [17] Y. Shiyang, Z. Xuecheng, Z. Zhige and C. Xiaofei. 2009. A Loop-Improved Capacitor-less Low-dropout Regulator for SoC Power Management Application. Asia-Pacific Conference on Power and Energy Engineering IEEE, pp. 1-4.
- [18] J. Hu, W. Liu and M. Ismail. 2010. Sleep-mode ready, area efficient capacitor-free low-drop-out regulator with input current-differencing. Analog Integr Circ Sig Process, vol. 63, no. 1, pp.107-112.
- [19] Z. Kamal, Q. Hassan and Z. Mouhcine. 2011. Full On-Chip Capacitance PMOS Low Dropout Voltage Regulator. IEEE International Conference on Multimedia Computing and systems in Morocco, vol. 54, no. 9, pp. 1-4.
- [20] D. Camacho, P. Gui and P. Moreira. 2010. Fully on-chip switched capacitor NMOS low dropout voltage Regulator. Analog Integr Circ Sig Process, vol.65, no. 1, pp.141–149.
- [21] C.-Chin Wang, R.-ChiKuo and T.-Han Tsai. 2011. A high precision low dropout regulator with nested feedback loops. Microelectronics Journal, vol.42, no.7, pp. 966–971.

AUTHOR'S PROFILE



Mr. Ashvani Kumar Mishra is currently pursuing M. Tech. (VLSI Design) in the Department of Electronics and Communication Engineering, Thapar University, Patiala. His research interests are analog and mixed-signal integrated circuit design.



Mr. Rishikesh Pandey is currently working as an Assistant Professor in the Department of Electronics and Communication Engineering, Thapar University, Patiala. His teaching and research areas are analog and digital VLSI design.