

HIGH SPEED CARRY SAVE MULTIPLIER BASED LINEAR CONVOLUTION USING VEDIC MATHAMATICS

M. Bharathi¹ D. Leela Rani² Prof. S. Varadarajan³

¹ Assistant Professor, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, India, bharathi891@gmail.com

² Associate Professor, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, India, dlrani79@gmail.com

³ Professor, Department of ECE, SVU College of Engineering, Tirupati. varadasouri@gmail.com

ABSTRACT

VLSI applications include Digital Signal Processing, Digital control systems, Telecommunications, Speech and Audio processing for audiology and speech language pathology. The latest research in VLSI is the design and implementation of DSP systems which are essential for above applications. The fundamental computation in DSP Systems is convolution. Convolution and LTI systems are the heart and soul of DSP. The behavior of LTI systems in continuous time is described by Convolution integral whereas the behavior in discrete-time is described by Linear convolution. In this paper, Linear convolution is performed using carry save multiplier architecture based on vertical and cross wise algorithm of Urdhva – Tiryagbhyam in Vedic mathematics. Coding is done using Verilog HDL(verilog Hardware Description Language). Simulation and Synthesis are performed using Xilinx FPGA.

Key words: Linear convolution, Urdhva - Tiryagbhyam, carry save multiplier, Verilog HDL.

1 INTRODUCTION

In this paper, carry save multiplier architecture is developed using Urdhva-Tiryagbhyam sutra. This sutra is applied to perform multiplication of size NXN.

Linear convolution which is a fundamental computation in Linear time-invariant (LTI) systems is implemented using Verilog HDL. Simulation and Synthesis are verified in Xilinx 10.1 ISE.

In general, multiplications are complex and slow in operation. The overall speed in multiplication depends on number of partial products generated, shifting the partial products based on bit position and summation of partial products. In carry save multiplier, the carry bits are passed diagonally downwards, which requires a vector merging

adder to obtain final sum of all the partial products[1]. In convolution, fundamental computations includes

multiplication and addition of input and impulse signals or samples[2].

2 CONVOLUTION

Linear and time-invariant systems are an important class of systems and has significant signal processing applications.

These systems obey linearity and time-invariance properties[3,4].

A Linear time invariant (LTI) system is completely characterized by its impulse. The impulse response is response of a system to impulse signal or sequence.

In continuous time, the linear time invariant system with input signal $x(t)$, output signal $y(t)$ and impulse response $h(t)$ are related by convolution integral.

$$y(t) = x(t) * h(t) = \int_{-\infty}^{\infty} x(t - \tau) h(\tau) d\tau$$

$$= \int_{-\infty}^{\infty} x(\tau) h(t - \tau) d\tau \quad (1)$$

$h(t)$ is the system's response to impulse $\delta(t)$.

$y(t)$ is therefore proportional to weighted average of input function $x(t)$. In general, every value of output depend on every value of input.

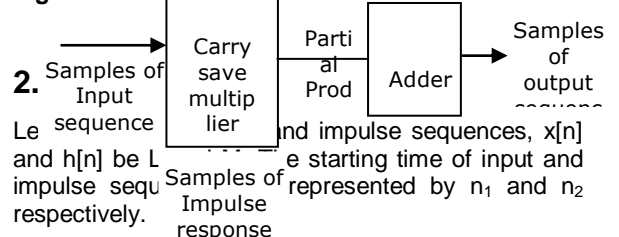
In discrete time, the output sequence $y[n]$ of a linear time invariant system, with impulse response $h[n]$ due to any input sequence $x[n]$ is the convolution sum of $x[n]$ with $h[n]$ and is given as

$$y[n] = x[n] * h[n] = \sum_{-\infty}^{\infty} x[k] h[n - k] \quad (2)$$

$h[n]$ is the response of the system to impulse sequence, $\delta[n]$.

To implement discrete time convolution, the two sequence $x[k]$ and $h[n-k]$ are multiplied together for $-\infty < k < \infty$ and the products are summed to compute output samples of $y[n]$. Convolution sum serves as an explicit realization of a discrete-time linear system. The above equation expresses each sample of output sequence in terms of all samples of input and impulse response sequence[5].

Fig 1: Block Diagram of Linear Convolution



Therefore, the length N, of output sequence
 $y[n] = L+M-1$

and the starting time $n = n_1 + n_2$

The samples of output sequence is computed using convolution sum

$$y[n] = \sum_{-\infty}^{\infty} x[k]h[n-k] \quad (3)$$

2.2 Example

Let the input sequence be $x[n] = \{1,2,3,4\}$

and impulse response, $h[n] = \{2,3,4,5\}$

Here, $L=4, M=4$. The length of the output Sequence
 $y[n], N=7$

$n_1 = 0, n_2 = 0$, The starting time of the output
sequence, is, $n=0$

The 1st sample with starting time $n=0$ is given by

$$y[n] = \sum_{-\infty}^{\infty} x[k]h[-k] \quad (4)$$

$$= x[0]h[0] + x[1]h[-1] + x[2]h[-2] + x[3]h[-3] = 2$$

Similarly, the other samples in the output sequence
are given by convolution sum as

$$y[1] = \sum_{-\infty}^{\infty} x[k]h[1-k] = 7$$

$$; y[2] = 16; y[3] = 30; y[4] = 34 ;$$

$$y[5] = 31; y[6] = 20$$

3 MULTIPLICATION TECHNIQUE

Jagadguru Swami Sri Bharati-Krishna Swamiji introduced his research on mathematics based on sixteen sutras for multiplication. A multiplier is the key block in Digital Signal processing. In the increasing technology, researchers are trying to design multipliers which offer high computational speed, less delay, low power and area efficient arithmetic building blocks[6].

In Linear Convolution, the multiplication is performed using Urdhva-Tiryagbhyam Sutra of Vedic mathematics[7]. The Comparison between number of multiplications and additions in Conventional Mathematical approach and vedic mathematics is shown. [8]

Example: Multiplication of 1234 and 2116

	1	2	3	4	
Adder	2	1	1	6	
Step1:	3	5	9	4	9
	0	0	1	2	2
	2	1	1	6	
	2	6	1	1	4

$4 \times 6 = 24$, 2, The carry is placed below the second digit

Step2:

1	2	3	4
		X	
2	1	1	6

$(3 \times 6) + (4 \times 1) = 22$. 2, the carry is placed below the third digit.

Step3:

1	2	3	4
		X	
2	1	1	6

$(2 \times 6) + (4 \times 1) + (3 \times 1) = 19$. 1, the carry is placed below the fourth digit.

Step4:

1	2	3	4
		X	
2	1	1	6

$(1 \times 6) + (2 \times 4) + (2 \times 1) + (3 \times 1) = 19$. The carry 1 is placed below the fifth digit.

Step5:

1	2	3	4
		X	
2	1	1	6

$(1 \times 1) + (3 \times 2) + (2 \times 1) = 9$. The carry 0 is placed below the sixth digit.

Step6:

1	2	3	4
		X	
2	1	1	6

$(1 \times 1) + (2 \times 2) = 5$. The carry 0 is placed below seventh digit.

Step7:

1	2	3	4
↓			
2	1	1	6

$(1 \times 2) = 2$.

4 SIMULATION RESULTS

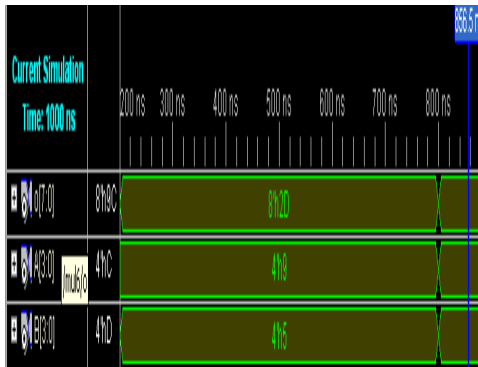


Fig 2: Adder output

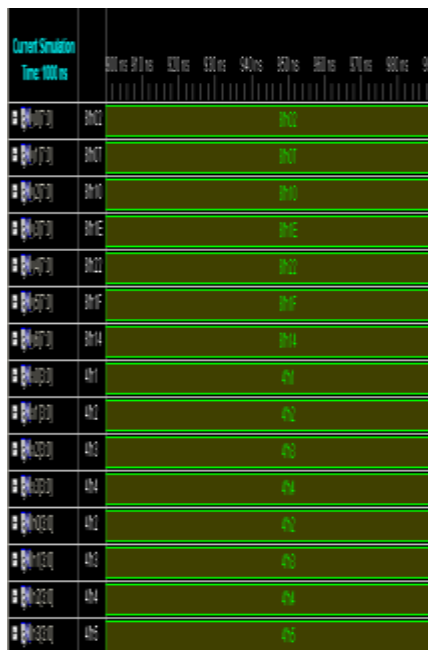


Fig 3: Convolution output



Fig 4: Convolution Block RTL

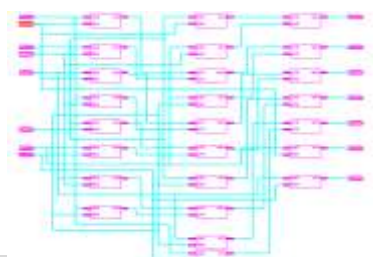


Fig 5: LUT Based RTL




5 CONCLUSION

In this paper, Linear convolution of discrete finite length sequences is performed using carry save multiplier based an Vedic sutra and an adder. The proposed multiplier using Vedic mathematics results in high computational speed and minimum critical path ,hence, less delay, when compared to simple multiplier. The maximum computational speed of Linear Convolution is 15.38 ns. The delay can further be reduced by optimizing adder.

REFERENCES

- [1] Jan M. Rabaey, Anantha Chandrasasan Borivoje Nikdic,2003, Digital Integrated Circuits-A Dexign perspective, Prentice-Hall.
- [2] Purushotam D. Chidgupkar and Mangesh T. Karad,2004, "The Implementation of vedic Algorithms in Digital Signal Processing", Global J. of Engng. Educ., Vol.8, No.2, UICEE Published in Australia.
- [3] J.G. Proakis and D.G. Monalkies,1988, Digital Signal Processing. Macmillian.
- [4] A.V. Oppenheim and R. Schafer, 1975, Discrete-Time Signal Processing Englewood Cliffs, NJ:Prentice-Hall.
- [5] Asmita Haveliya, Kamlesh Kumar Singh,2011, "A Novel Approach For High Speed Block Convolution Algorithm", proc. Of the International Conference on Advanced Computing and Vommunication Technologies (ACCT).
- [6] Jagadguru Swami Sri Bharati Krishna Tirthji Maharaja,1986, "Vedic Mathematics", Motilal Banarsidas, Varanasi, India.
- [7] Human Tharafu M.C. Jayalaxmi. H. Renuka R.K., Ravishankar. M.,2007, "A. high speed block convolution using Ancient Indian Vedic Mathematics", IEEE International conference on computational intelligence and multimedia applications.
- [8] A.P. Nicholas, K.R Willaiams, J. Pickles, 2003, Vertically and Crosswise applications of the Vedic Mathematics Sutra, Motilal Banarsidass Publishers, Delhi.

BIO-DATA

	<p>Ms.M.Bharathi, M.Tech., is currently working as an Assistant Professor in ECE department of Sree Vidyanikethan Engineering College, Tirupati. She has completed M.Tech in VLSI Design, in Satyabhama University. Her research areas are Digital System Design, VLSI Signal Processing</p>
	<p>Ms.D.Leela Rani received the M.Tech. degree from Sri Venkateswara University, Tirupati. She is currently working towards the Ph.D. degree in the Department of Electronics and communication Engineering, SVU College of Engineering,Tirupati. Currently she is working as an Associate professor in Sree Vidyanikethan Engineering College (Autonomous). Her research areas include, Atmospheric Radar Signal Processing and VLSI Signal Processing.</p>
	<p>Prof.S.Varadarajan did his M.Tech from NIT,Warangal, India and Ph.D from Sri Venkateswara University. His specializations include Signal Processing and Digital Communications. He is working as Professor in the department of Electronics and Communication Engineering, Sri Venkateswara University College of Engineering, Tirupati, India. He is a fellow of Institution of Electronics and Telecommunication Engineers, India and member of IEEE.</p>