



## Comparative Analysis Domino Logic Based Techniques For VLSI Circuit

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### ABSTRACT

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. Domino logic technique is widely used in modern digital VLSI circuit. Dynamic logic is twice as fast as static CMOS logic because it uses only N fast transistors. The Dynamic (Domino) logic circuit are often favored in high performance designs because of the high speed and low area advantage.

Four different dynamic circuit techniques including Basic domino logic circuit are compared in this paper for low power consumption and speed of domino logic circuits. For digital circuit simulation used BSIM (Berkeley Short Channel IGFET) Model because it control leakage current.

### Indexing terms/Keywords

Domino logic circuit; domino logic with keeper; High speed and leakage Tolerant Domino; Low Swing Domino.

### SUBJECT CLASSIFICATION

VLSI.

### TYPE (METHOD/APPROACH)

Simulation based comparative study.

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## INTRODUCTION

To achieve low power and speed different size of transistor and supply voltages are scaled down along with different technology. Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [1]-[2].

The domino logic with keeper technique have feedback keepers were proposed to prevent the dynamic node from floating; internal nodes were precharged to eliminate the charge sharing problem; and weak complementary p-network is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates.

The High speed and leakage Tolerant Domino Technique add a footer transistor that is initially OFF in the evaluation phase to reduce leakage and then turned ON to complete the evaluation. In order to avoid the delay penalty due to an initially OFF footer transistor, an extra path for evaluation is provided that is controlled by the output[4]. This technique reduce the contention current between keeper transistor and NMOS transistor in evaluation phase. This circuit increase speed and decreases the power dissipation of the circuit as compared to other domino logic styles.

The low swing domino logic technique is decrease the power consumption without sacrificing the noise immunity. The voltage swings at the nodes of domino logic circuits are modified.[11]

## Domino Logic Techniques

### A. Basic Domino Logic

Domino CMOS was proposed in 1982 by Krambeck. It has same structure as dynamic logic gates, but adds static buffering CMOS inverter to its output. The introduction of the static inverter has the additional advantage of the output having a low-impedance output, which increases noise immunity and drives the fan-out of the gate. The buffer furthermore reduces the capacitance of the dynamic output node by separating internal and load capacitance. The buffer itself can be optimized to drive the fan-out in an optimal way for high speed. This logic is the most common form of dynamic gates, achieving a 20% to 50% performance increase over static logic [3].

In Basic Domino logic family evolved from PMOS and NMOS transistors and therefore retained two phase of operation. A single clock is used to both precharge and evaluation phase. This circuitry incorporates a static CMOS buffer into each logic gate as shown in Figure.1 During the precharge phase input is low (CLK=0), PMOS transistor is ON and NMOS transistor is OFF, Node  $V_o$  is charged up to  $V_{dd}$  and the output from the inverter is at close to the 0 voltage level. In this phase no path between pull down network to  $V_o$ . [9]

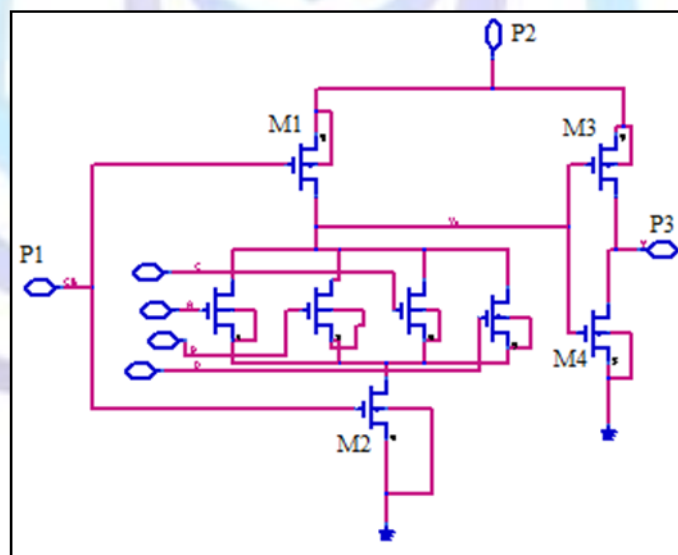


Figure1:Basic Domino logic circuit

Next, during the evaluation phase, NMOS transistor is ON creating the path node  $V_o$  through to pull down network to the ground. Node  $V_o$  is discharged and inverter make output one.. It should be noted that in Domino logic the transition of nodes Y is always from low to high and it is rippled through the logic from the primary inputs lo the primary outputs.

### B. Domino Logic Circuit with keeper

The Keeper technique improves the noise immunity and avoid the problem of charge sharing of Domino logic circuit.

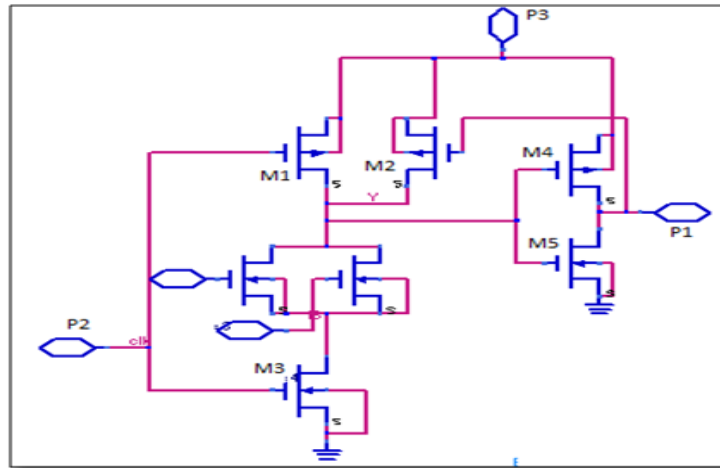


Figure.2. Domino logic circuit with keeper

The keeper is a weak pMOS transistor that holds the output at the correct level when it would otherwise float. When the dynamic node is high, the output is low and the keeper is ON to prevent from floating (Figure.2). When the dynamic node (Y) falls, the keeper initially opposes the transition so it must be much weaker than the pull down network. Eventually Z rises, turning the keeper OFF and avoiding static power dissipation.

The keeper must be strong enough to compensate for any leakage current drawn when the output is floating and the pull down stack is OFF.

If increase the width of keeper transistor then increase delay, so keeper transistor are order of 1/10 the strength of the pull down stack.[5]

### C. High Speed Leakage Tolerant Domino

The HSLTD circuit scheme is shown in Figure3. Transistor M3 is used as stacking transistor. Due to voltage drop across M3, gate-to-source voltage of the NMOS transistor in the PDN (Pull down network) decreases. M7 causes the stacking effect and makes gate-to-source voltage of M6 smaller (M6 less conducting). Hence circuit becomes more noise robust and less leakage power consuming. But performance degrades because of stacking effect in mirror current path. This can be increased by widening the M2 (high W/L) to make it more conducting.[6]

if there is noise at the inputs at the onset of evaluation, the dynamic node can be discharged resulting in wrong evaluation.

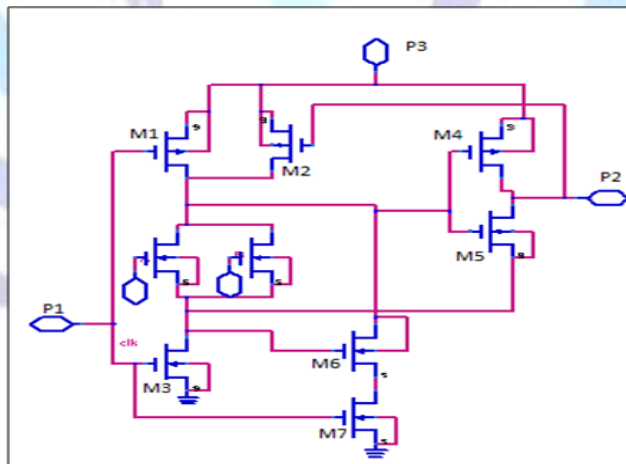


Figure3: High speed leakage tolerant Domino

### D. Low Swing Domino Logic

Low swing domino technique applied to reduce dynamic switching power. Two techniques are under the low swing domino circuit. The first technique is low swing domino with fully driven keeper (LSDFDK). The output voltage swing between ground and  $V_{DD}-V_{in}$ . And second is low swing domino circuit with weakly driven keeper (LSDWDK).

These techniques reduce the voltage swing at the output node using the NMOS transistor as a pull up transistor. The first technique is improved the delay and power while maintaining robustness against noise. The second technique reduces the contention current by reducing the gate voltage swing of keeper transistor. LSDWDK generate two different voltage swings. The output voltage swing between ground and  $V_{DD}-V_{in}$ . The gate voltage swing between  $|V_{tp}|$  and  $V_{DD}$ [2].

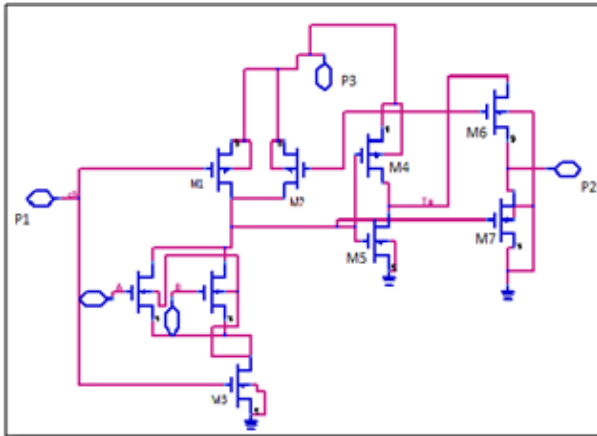


Figure:4.a LSDFDK

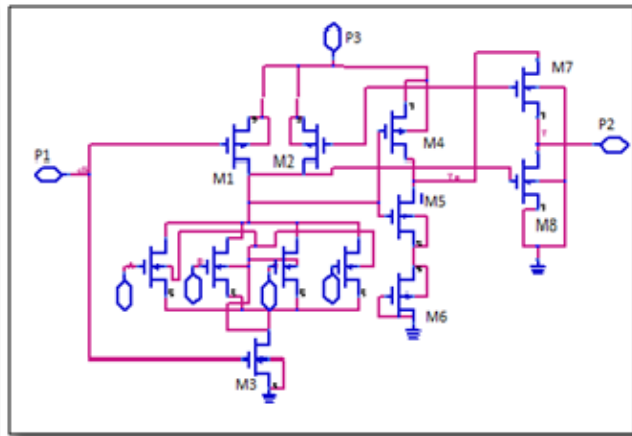


Figure:4.b: LSDWDK

**Figure: 4: Low swing domino logic circuit**

## Power Dissipation

The power consumed by CMOS circuit classified in two type.

- Static power dissipation
- Dynamic power dissipation
  - i. Static Power Dissipation:- This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. static power dissipation in CMOS inverter is negligible.[6]
  - ii. Dynamic Power Dissipation:-The PMOS and NMOS transistors are on during the perform operation simultaneously. the duration of changing inputs low to high and discharging high to low pMOS and nMOS turn on respectively. During this time a current flows between Vdd to GND (make short path) and Dynamic Power produce. The dynamic power dissipation is proportional to the square of voltage supply.[7-8]

## Noise

The noise is unwanted signal which generate in circuit cause of corrupt part of system. The noise can be internal or external noise of the system.

- i. Charge sharing noise is produce caused by charge redistribution.
- ii. Leakage noise are the possible charge loss in theevaluation phase.
- iii. Input noise are noise presented at the inputs of alogic gate.
- iv. Power and ground noise is generate caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package.

The noise tolerance for digital circuit is called noise margin, and the noise immunity of the circuit increases with noise margin [8].

## Propagation Delay

The propagation delay  $t_m$   $T_{PHL}$  and  $T_{PLH}$  find out the input to output signal delay during high to low and low to high transition on the output.

$T_{PHL}$  equal to time delay between  $V_{50\%}$  transition of the rising input voltage and  $V_{50\%}$  transition of the falling voltage output.

$T_{PLH}$  equal to the time delay between  $V_{50\%}$  transition of the falling input voltage and  $V_{50\%}$  transition of the rising voltage output.

## Simulation and Result

In this work, the benchmark circuits using the stated four techniques are implemented. The figures of merits used to compare these techniques are power consumption, propagation delay and power delay product (PDP). The benchmark circuits implemented are OR gate for 4 input and 6input as well as AND gate for 4 input and 6input . These design styles are compared by performing detailed transistor-level simulations on benchmark circuits using Advance Design System (ADS). The results of the benchmark circuits for all techniques are given below. Table1 shows the comparison of all the for techniques for four input OR gate. Table2 shows the comparison of all the four techniques with that of standard domino



circuit for six input OR gate. Table 3 shows the comparison of all the four techniques for four input AND gate. Table 4 shows the comparison of all the four techniques with that of standard domino circuit for six input AND gate.

From the results, it can be observed that the Domino logic techniques, viz., Basic domino logic circuit, Domino logic circuit with keeper, High speed leakage tolerant domino and Low Swing Domino techniques provide lower values of power dissipation, propagation delay and PDP. The propagation delay (Tpd-Sec), power consumption (Pavg-Watt) and power delay product (PDP-Watt-Sec) calculated.

**Table.1: four input OR gate**

Technique	Tpd	Pavg	PDP
Domino	1.34E-08	4.45E-06	5.94E-14
Keeper	3.40E-09	5.56E-06	1.51E-14
HSLDT	3.19E-09	7.38E-06	3.29E-14
LSDFDK	3.40E-09	1.04E-05	3.53E-14

**Table.2: six input OR gate**

Technique	Tpd	Pavg	PDP
Domino	3.66E-09	6.50E-06	1.90E-14
Keeper	3.65E-09	6.50E-06	1.89E-14
HSLDT	3.85E-09	1.24E-06	4.78E-14
LSDFDK	3.84E-09	1.16E-06	4.44E-14

**Table.3: four input AND gate**

Technique	Tpd	Pavg	PDP
Domino	1.30E-10	5.29E-06	6.89E-16
Keeper	2.85E-10	2.42E-06	6.89E-16
HSLDT	1.53E-10	5.35E-06	8.20E-16
LSDFDK	2.88E-09	6.68E-06	1.92E-14

**Table.4: six input AND gate**

Technique	Tpd	Pavg	PDP
Domino	2.23E-09	1.44E-06	2.52E-15
Keeper	1.59E-09	1.44E-06	1.83E-15
HSLDT	1.99E-09	1.90E-06	5.28E-15
LSDFDK	1.74E-09	2.53E-06	5.29E-15

## CONCLUSION

In this work, an attempt had been made to simulate OR gate and AND gate for four and six inputs by using four domino based techniques including basic (standard domino). The comparative analysis showed the maximum number (six) of input for OR gate low swing domino with fully driven keeper [LSDFDK] technique is better because it had low power consumption, low propagation delay but domino logic with keeper had less PDP.

The comparative analysis for 4 input OR gate showed LSDFDK had less power compare to other techniques, standard domino had less Tpd and domino logic keeper had low PDP compared to other domino techniques.

The comparative analysis showed the maximum number (six) of input for AND domino logic keeper technique is better because it had low power consumption, low propagation delay and less PDP.

Similarly comparison for the four input AND gate showed domino logic keeper had less power and low PDP compare to other techniques and standard domino had less Tpd compared to other domino techniques.



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