FPGA IMPLEMENTATION OF INTELLIGENT EMBEDDED SYSTEM FOR DISTRIBUTED ELECTRICAL APPLIANCES

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ABSTRACT

Now a days, Technology is very important in daily life. In the offices, the usage of electronic appliances is increasing rapidly. So the demand for power is also increasing. The power demand can be met upto some extent by reducing power wastage. The proposed system reduces power wastage by switching off the electrical appliances when not in use. The proposed system controls the appliances automatically based on the need and is implemented on FPGA in Xilinx platform using Verilog HDL.

Keywords: power,FPGA

I.INTRODUCTION

There are various monitoring and control systems like Home security monitoring and control system[1], Street light monitoring and control system, Railway monitoring system, Temperature monitoring system, Patient monitoring system etc., for different purposes.
All these systems are embedded systems in different fields. In industry, there is one system called intelligent embedded system for distributed electrical appliances. This system is focused in this paper. The explanation is given below.

In the offices, employees left their rooms without switching off the electrical appliances. So the power wastage increases. To avoid power wastage, the existing system monitors and controls the electrical appliances automatically based on the requirement. The existing system[2] uses Zigbee modem for communication and Remote control unit to control the appliances. Basically Zigbee is used for long distance communication in wireless communication. Bluetooth and Infrared can't be used for long distance communication. Zigbee builds upon physical layer and medium access control layer defined in IEEE 802.15.4 for low-rate WPANs[3][4]. The technology defined by the Zigbee specification is intended to be simpler and less expensive than other WPANs such as Bluetooth. Zigbee provides secure networking and it has data rate of 250Kbps. The existing system is implemented using Keil software. The existing system uses more hardware and we can't add new features to the system. The proposed system which is implemented on FPGA acheives reconfigurability.

In this system Zigbee modem has to be implemented on FPGA. So study of different modems implemented on FPGA is necessary[5][6][7][8].

II.PROPOSED INTELLIGENT EMBEDDED SYSTEM

Fig. 1 Shows the block diagram of Intelligent embedded system. This system is meant for industry applications i.e., mainly in the offices. In Fig. 1 the PC(personal computer) transmits the necessary information through modem. Personal computer controls the electrical appliances with the help of modems and remote control unit. In Fig. 1 "loads" indicate the electrical appliances. The system uses four modems. One modem is placed at the transmitter and remaining 3 modems are placed at receivers in 3 floors. Zigbee modems are used to provide communication for long distance. Zigbee modem uses Offset-Qpsk modulation and Offset-Qpsk demodulation techniques[9] for transmission and reception. These techniques have some advantages when compared to remaining techniques. The purpose of modem is to transmit and receive the necessary information to control the electrical appliances automatically. The purpose of remote control unit is to control the electrical appliances.

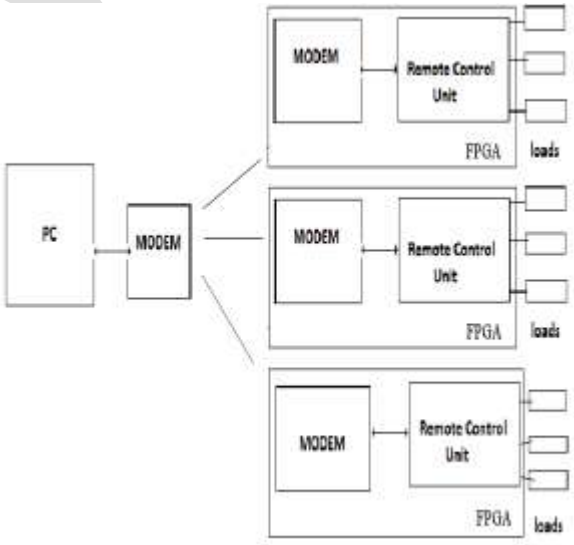

Fig. 1: Block diagram of proposed Intelligent embedded system

The system is designed for 3 floors in the office. To control the electrical appliances automatically, the system has zigbee modems at both transmitter and receiver. The zigbee modem at personal computer will send the necessary information to each floor. One RCU(Remote Control Unit) is placed in each floor. Each RCU can control 16 electrical appliances and each RCU is given unique ID. Actually the information will be transmitted to the 3 floors. In the each floor, RCU checks input message whether the received command belongs to the corresponding floor or not. If ID matches with 1st floor, the appliances in the 1st floor can be controlled. The electrical appliances may be of any kind like lights,fans,air conditions etc.,

If employees do not switch off ACs, lot of power will be wasted because it consumes more power than any other electrical appliances. So this system saves lot of power by switching off the appliances automatically.

III.IMPLEMENTATION:

Algorithm for top level module of Intellegent embedded system:

Step1:Start

Step2:Define inputs and outputs

Step3:Call the transmitter function to establish communication

Step4:Call the receiver1 function and check whether ID matches with first floor or not

Step5:Call the receiver2 function and check whether ID matches with second floor or not

Step6:Call the receiver3 function and check whether ID matches with third floor or not

Step7:Control the appliances in the particular floor

Step8:Stop

In the algorithm, after defining inputs and outputs transmitter function will be called to transmit the information. The necessary information will be transmitted from transmitter to all the receivers. Each receiver checks ID and the appliances in the corresponding floor can be controlled.

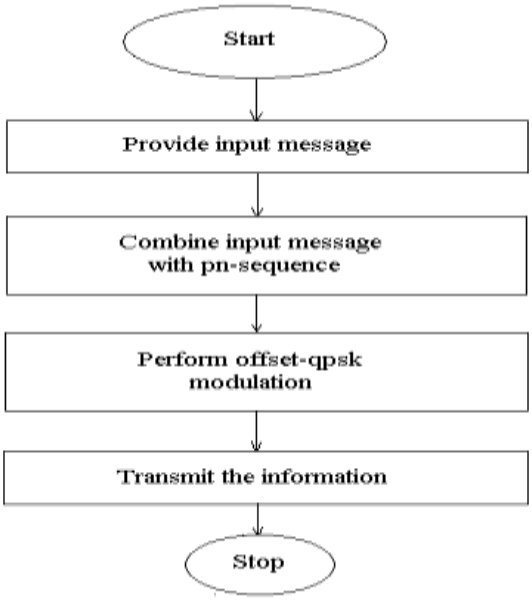

Fig. 2: Flowchart of modem transmitter

Fig. 2 shows the flowchart of modem transmitter. In Fig. 2 the input message is combined with pseudo noise sequence.

The input message comes from personal computer. The Psuedo noise sequence is generated by Linear feedback shift register. The resultant data is called scrambled data. The scrambled data is modulated using Offset-QPSK modulation technique. After modulation, the data is ready for transmission.

Fig. 3 shows the flowchart of modem receiver. In Fig. 3 the received information is demodulated using Offset-QPSK demodulation. The resultant data is combined with Psuedo-noise sequence to extract the original message. The floor ID is checked in the original input message to control the appliances because the first 16 bits original input message represent floor ID. Each receiver checks input message. If floor ID matches with first floor, the appliances in the first floor can be controlled.

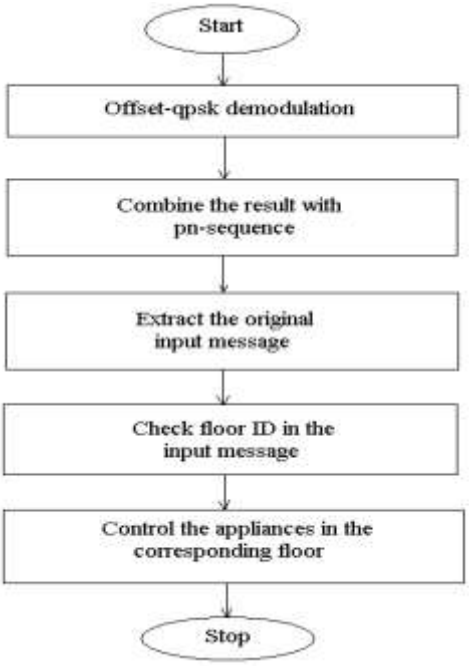

Fig. 3: Flowchart of modem receiver

IV.RESULTS:

The code is written in Verilog HDL using Xilinx platform. The simulation results are obtained in case of 3 receivers in 3 floors. Schematics are obtained to observe the internal structure of the system.

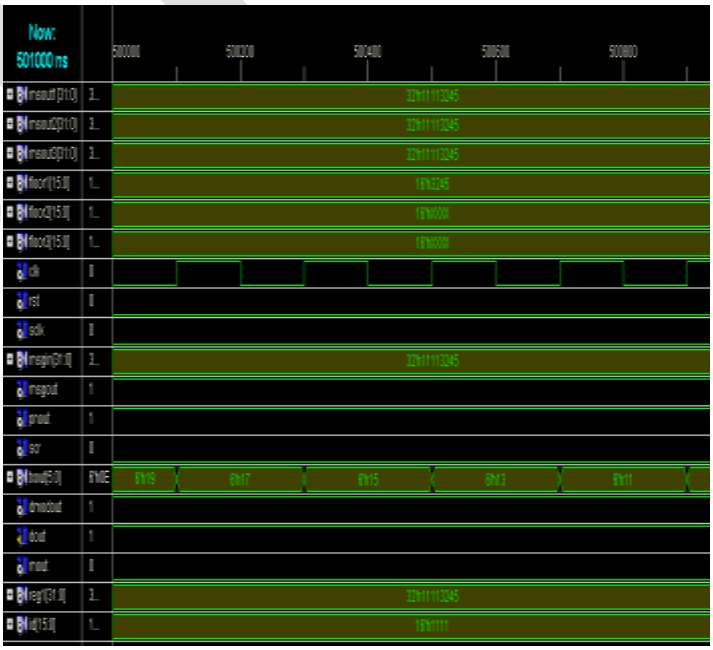

Fig. 4A: Simulation result when controlling the appliances of first floor

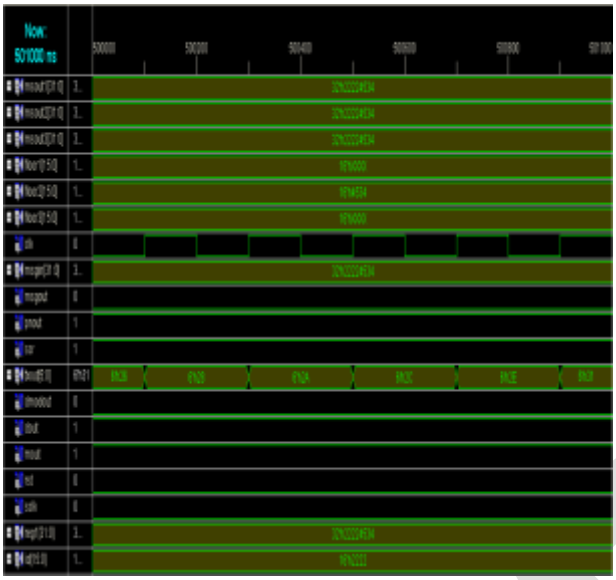

Fig. 4B: Simulation result when controlling the appliances of second floor

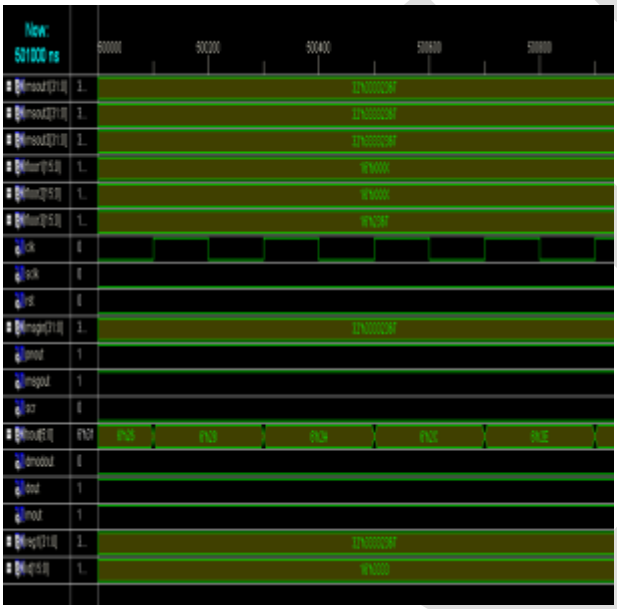

Fig. 4C: Simulation result when controlling the appliances of third floor

In the figures 4A,4B,4C , "msgin[31:0]" is 32-bit input data which is in parallel form. This parallel data is converted into serial form. The resultant output is "msgout". "Pnout" represents pseudo-noise sequence. After multiplying 'msgout' and 'pnout' we will get the scrambled data i.e., "scr". After performing Offset-qpsk modulation of scrambled data we get "txout". Now the 'txout' will be transmitted. The receiver receives 'txout' . Demodulation of 'txout' results in "dmodout". The 'dmodout' will be multiplied with pn-sequence to get "mout". After converting 'mout' into parallel data, we get "msout1[31:0]". This will be copied into a register called "reg1[31:0]". First 16 bits represent 'floor id' and remaining 16 bits can be used to control the 16 electrical appliances.

In Fig. 4A the first 4 digits of hexadecimal number i.e., '1111' represent first floor. So the appliances of first floor can be controlled. In Fig. 4B the first 4 digits of hexadecimal number i.e., '2222' represent second floor. So the appliances of second floor can be controlled. In Fig. 4C the first 4 digits of hexadecimal number i.e., '3333' represent third floor. So the appliances of third floor can be controlled.

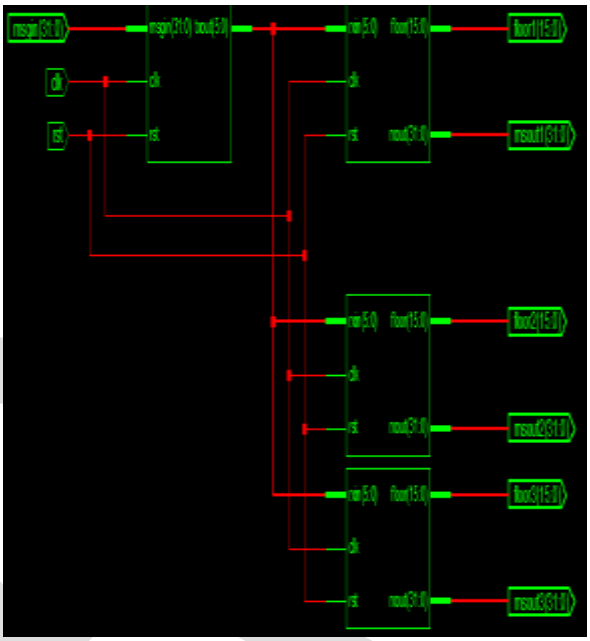

Fig. 5: RTL Schematic of Intellegent embedded system

Fig. 5 shows the RTL Schematic of Intellegent embedded system. In Fig. 5 "msgin" stands for input message and "txout" stands for output of transmitter. Output of transmitter will be sent to 3 receivers i.e., to the "rxin" pin of receivers. After performing demodulation and some other operation, we get "rxout". Now floor ID will be checked because message also contains floor ID. The appliances in the particular floor can be controlled. The resultant output is "floor(15:0)". The clock input is used to perform the task at raising edge of the clock pulse. The "rst" pin is used to reset the system operation. The 'clk' input and 'rst' inputs are comman for all the blocks. The transmission of information is clear in the above diagram. The task of comparing floor ID and modem receiver are combined in the blocks shown at the receiver side. The block shown at the transmitter side acts as modem transmitter.

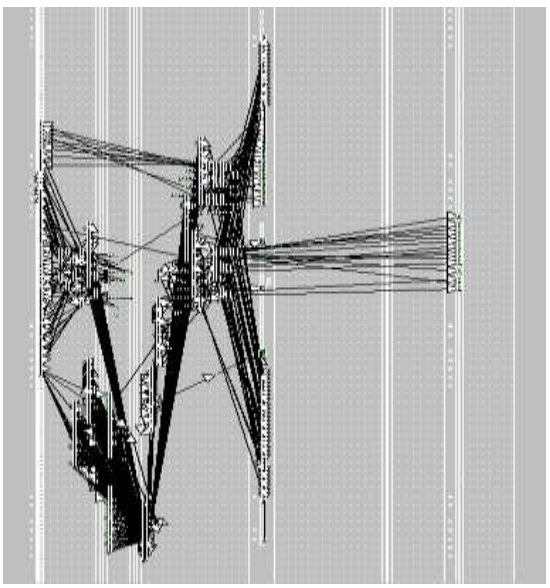

Fig. 6: Place and Route diagram

All signals are completely routed in the design.

The Average connection delay for this design is: 0.595ns. This design has maximum pin delay of 2.617ns and average connection delay on the 10 worst nets is of 2.416ns.

SYNTHESIS REPORTS

```
Synthesizing Unit <top>.
    Related source file is "top.v".
Unit <top> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# ROMs                                  : 1
 64x6-bit ROM                          : 1
# Adders/Subtractors                    : 1
 6-bit adder                           : 1
# Counters                              : 12
 32-bit up counter                     : 12
# Registers                             : 135
 1-bit register                        : 124
 16-bit register                       : 3
 32-bit register                       : 3
 6-bit register                        : 5
# Xors                                  : 8
 1-bit xor2                            : 8

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Advanced HDL Synthesis Report

Macro Statistics
# ROMs                                  : 1
 64x6-bit ROM                          : 1
# Adders/Subtractors                    : 1
 6-bit adder                           : 1
# Counters                              : 11
 32-bit up counter                     : 11
# Registers                             : 297
 Flip-Flops                            : 297
# Xors                                  : 8
 1-bit xor2                            : 8

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System is operating at clock frequency of 148.500MHZ. Transmitter operates with 848.176MHZ and Receivers are operating with 291.587MHZ. Total memory used for this design is 321084 kilobytes.

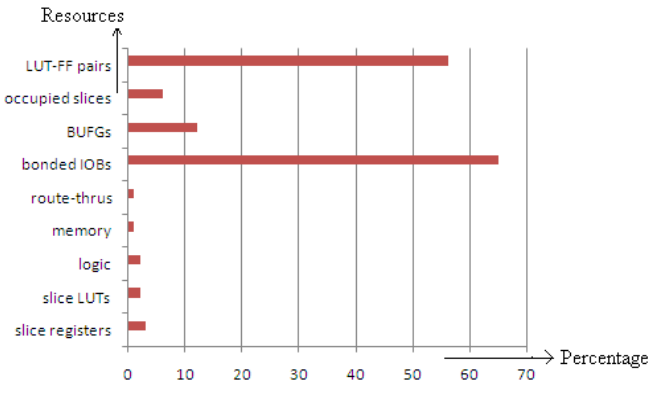

Fig. 7: Utilization of FPGA resources

Fig. 7 illustrates the utilization of FPGA resources interms of percentage. From this information we can understand how the system is occupying the resources of FPGA. Resources of FPGA include LUTs,FFs,IOBs,etc.,

Proposed Intelligent embedded system is consuming the power of 356mw and is operating at a clock frequency of 148.500MHZ. The gate count for the design is 8,924.

CONCLUSION

In this system, power wastage is reduced by keeping the appliances in off mode while not in use. Existing system uses one analog component called zigbee modem, micro controller, other ICs for different tasks. Once the existing system is programmed, it can't be modified. The proposed system implements all components on single FPGA chip. So it saves lot of hardware. Because of FPGA chip, it achieves reconfigurability.

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