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# Cost Analysis and Simulation of Decimator for Multirate Applications

Rajesh Mehra, Lajwanti Singh
Department Of Electronics & Communication, NITTTR, Chandigarh
rajeshmehra@yahoo.com
Department Of Electronics & Communication, AICE, Jaipur
lajwanti.singh@anandice.ac.in

## ABSTRACT

In this paper, a decimator design has been presented for multirate digital signal processing. The decimator design has been analysed and simulated for cost comparison in terms of multipliers and MPIS. Two structures namely Transposed Direct form and Symmetric Direct form have been used performance and resource consumption analysis. The decimators have been designed & simulated using MATLAB. It can be observed from the simulated results that symmetric structure comsumes almost 50% less multipliers and MPIS compared to transposed structure. So the symmetric structure based decimator is suitable to provide cost effective solution Keywords

DA, Decimator, DSP, FIR, FPGA

## Academic Discipline And Sub-Disciplines

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## SUBJECT CLASSIFICATION

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## TYPE (METHOD/APPROACH)

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## 1. INTRODUCTION

The demands for digital products with programmability are growing day by day. Various industries like audio, video, and cellular industry rely heavily on digital technology. There is a trend in the current design of DSP wireless communication circuits such as digital receivers to implement the whole receiver as an all digital, single - chip ASIC and to push the signal processor closer to the "front end" (of antenna or sensor). One of the main implications of this trend is the need for flexibly programming or configuring hardware so that it can accommodate multiple communication standards. A digital implementation keeps the IC manufacturing cost low while still providing the same performance as an analog implementation. A great part of digital technology deals with digital signal processing. This aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology.

Finite impulse response (FIR) digital filters are common DSP functions and are widely used in FPGA implementations. If very high sampling rates are required, full-parallel hardware must be used where every clock edge feeds a new input sample and produces a new output sample [1]. In case fully parallel implementation is not possible then partly serial approach can be adopted to enhance the system performance. Such filters can be implemented on FPGAs using combinations of the general purpose logic fabric, onboard RAM and embedded arithmetic hardware. Therefore, power consumption has resulted to be the most significant design requirement in portable systems and this has lead to many low power design techniques and the algorithms are used for speed and area optimization.

The key advantage to the approach is Cost:

1. Price for high speed components goes up exponentially with sample rate or clock rate.
2. Break the processing into parallel stages operating at a lower rate.

Different approaches of number representation are implemented on Decimation (reduction of sample rate) which is useful for:

1. Increase effective resolution of A/D.
2. Reduce data for processing.
3. Create low computational count narrowband filters.
4. Perform frequency translation.
5. Divide a wide band into narrow independent channels
6. Relax requirement on anti-aliasing filtering.

## 2. Multirate Digital Signal Processing

Multirate DSP hardware is an important sub-category of the DSP hardware. It deals with the sampling rate conversion of a digital signal, including interpolation and decimation. There are basically two methods to accomplish this. One method converts a digital signal to analog through a digital to analog convertor, and then re-samples the analog signal using a different sampling rate with an analog to digital convertor, a process that requires analog filters. The other method operates totally in the digital domain, which has a great advantage over the first method as only digital filters are needed [2].

One of the typical applications for decimation filters in telecommunications is a digital receiver. A digital receiver is more complex than an analog receiver, since the RF signal is transferred to digital domain and then back to analog domain after being processed. Why is a complex structure preferred? One reason is that digital filters have certain advantages over analog filters in terms of performance, implementation cost, and long term stability. Another is that the precision of many parameters cannot be easily controlled for the analog manufacturing process, while it is possible to implement digital filters with well controlled features such as small pass band ripple, sharp transition band characteristics and linear phase. The high frequency components need to be eliminated, and the unnecessarily high sampling rate needs to be brought down since the sampling rate only needs to be greater than twice the bandwidth of the signal .The decimation filter eliminates frequency components beyond baseband and reduces the sampling rate down to Fs/N. Then the signal with the low sampling rate is ready to be processed by the DSP processor.

## 3. FIR FILTER

FIR filter is a finite impulse response filter which are non- recursive in nature. That is, there is no feedback involved. The impulse response of an FIR filter will eventually reach zero. FIR filter is stable and has linear phase. It depends only on inputs and consist of only zeroes [3]. FIR filters are filters having a transfer function of a polynomial in *z*- and is an all-zero filter in the sense that the zeroes in the *z*-plane determine the frequency response magnitude characteristic.

### 3.1 FIR Filter Structures

Different type of structures are available for FIR filters:

1. Direct Form  2. Transposed Form  3. Symmetric Form

Figure 1 shows the structure of the Direct Form. The input is delayed, multiplied with the right values of the impulse response and then summed up to form the output [4].

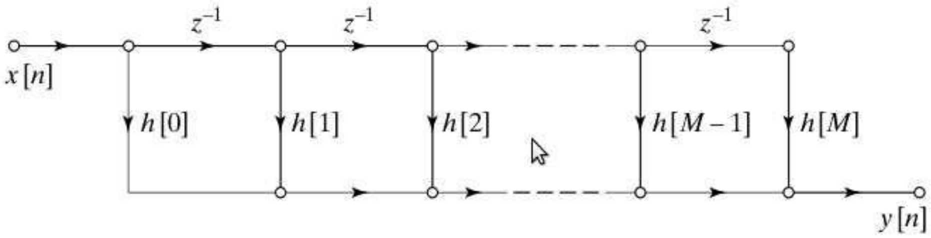



Fig 1: Direct form FIR filter structure [4]

A variation of the direct FIR model is called the transposed FIR filter. It can be constructed from the FIR filter by exchanging the input and output andinverting the direction of signal flow. In this form, the multiplication with the values of the impulse response is done before delaying. After each delay a temporary sum is calculated until the output is reached. Functionality wise the transposed structure is same as direct form structure as the impulse response is same for both. Hence the transposed form filter behaviour is same as direct form for any input [5].

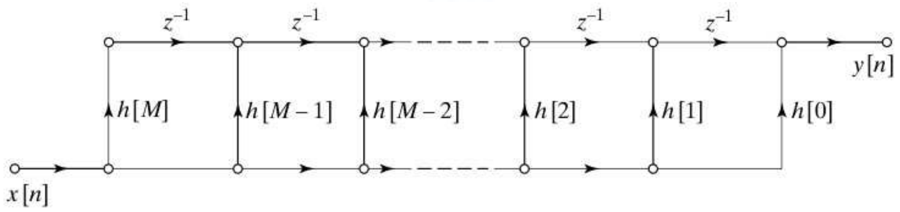



Fig 2: Transposed form FIR filter structure [5]

The symmetry (or antisymmetry) property of a linear-phase FIR filter can be exploited to reduce the number of multipliers into almost half of that in the direct form implementations [6].

## 3. DECIMATOR

Typically low pass filters are used to reduce the bandwidth of a signal prior to reducing the sampling rate. This is done to minimize aliasing due to the reduction in the sampling rate. Down sampler is basic sampling rate alteration device used to decrease the sampling rate by an integer factor [6].

In signal processing, down sampling (or "sub sampling") is the process of reducing the sampling rate of a signal. This is usually done to reduce the data rate or the size of the data. The down sampling factor (commonly denoted by M) is usually an integer or a rational fraction greater than unity. This factor multiplies the sampling time or, equivalently, divides the sampling rate. One simple way of decimating a digital signal x(n) by a factor of M is to select every Mth sample of the input signal x(n).

An down sampler with a down-sampling factor *M*, where *M* is a positive integer, develops an output sequence *y*[*n*] with a sampling rate that is (1/*M*)th of that of the input sequence *x*[*n*].

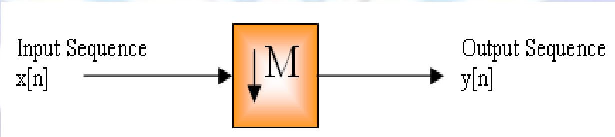


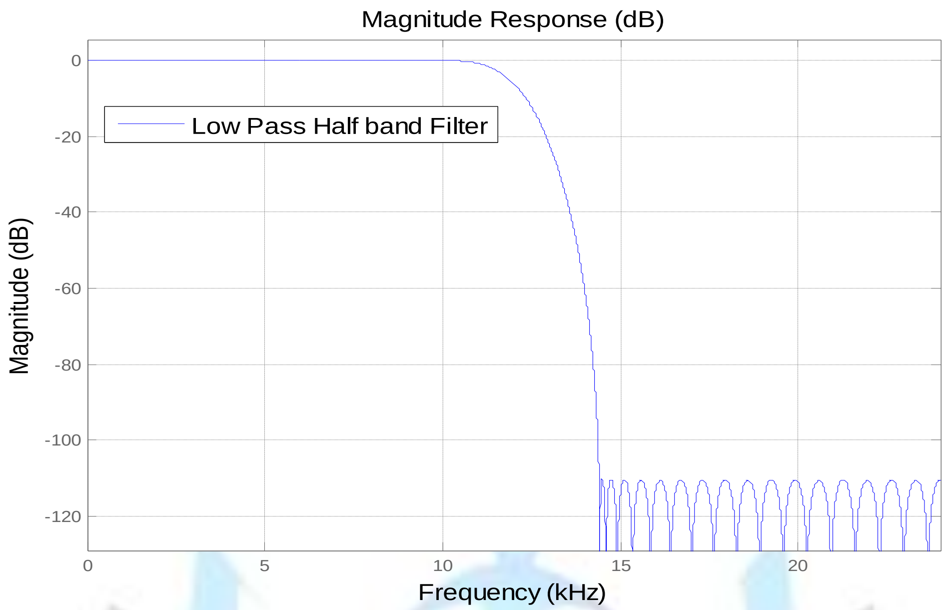

Fig 3: Down Sampling

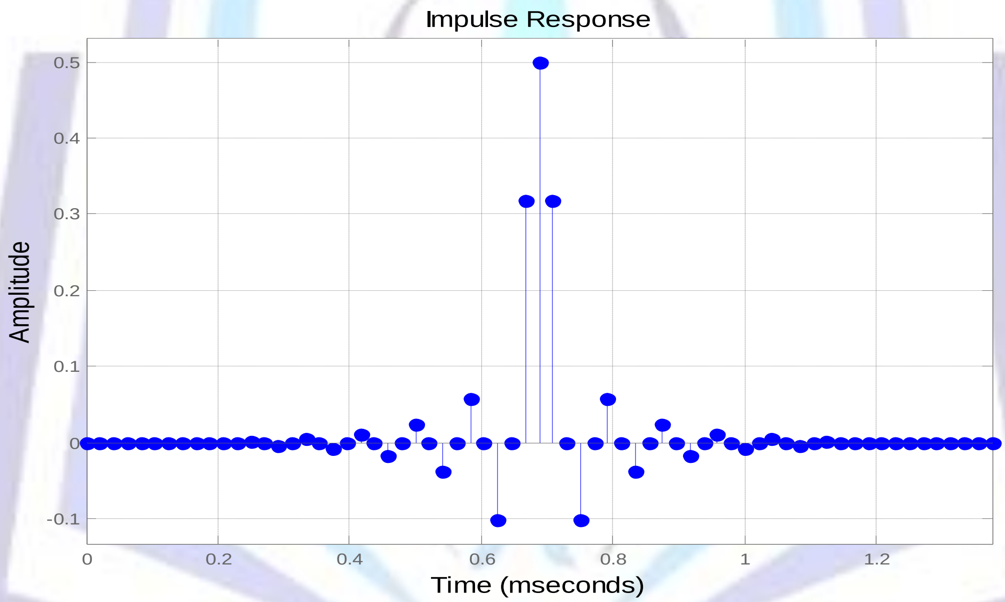
Down-sampling operation is implemented by keeping every Mth sample of x[n] and removing M-1 in-between samples to generate y[n]. The input and output relation of down sampler can be expressed as [7]:

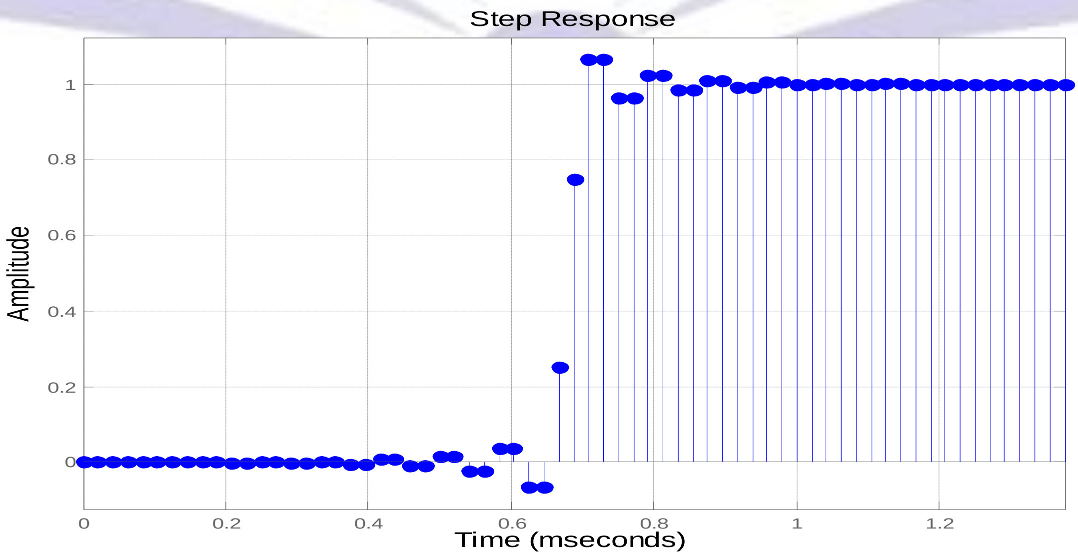
$y[n] = x[nM]$

## 4. PROPOSED DESIGN SIMULATION

The 66 tap FIR filter has been developed and compared for different FIR structures. Equiripple based Symmetric FIR filter compared with Transposed Direct form structure which is analyzed and designed using Matlab7.008 .The main advantage of Direct form Symmetric FIR is that it requires less number of multipliers and multiplier per input sample.


Magnitude Response (dB)
Low Pass Half band Filter
Magnitude (dB)
0
-20
-40
-60
-80
-100
-120
0
5
10
15
20
Frequency (kHz)


Impulse Response
Amplitude
0.5
0.4
0.3
0.2
0.1
0
-0.1
0
0.2
0.4
0.6
0.8
1
1.2
Time (mseconds)


Step Response
Amplitude
1
0.8
0.6
0.4
0.2
0
0
0.2
0.4
0.6
0.8
1
1.2
Time (mseconds)

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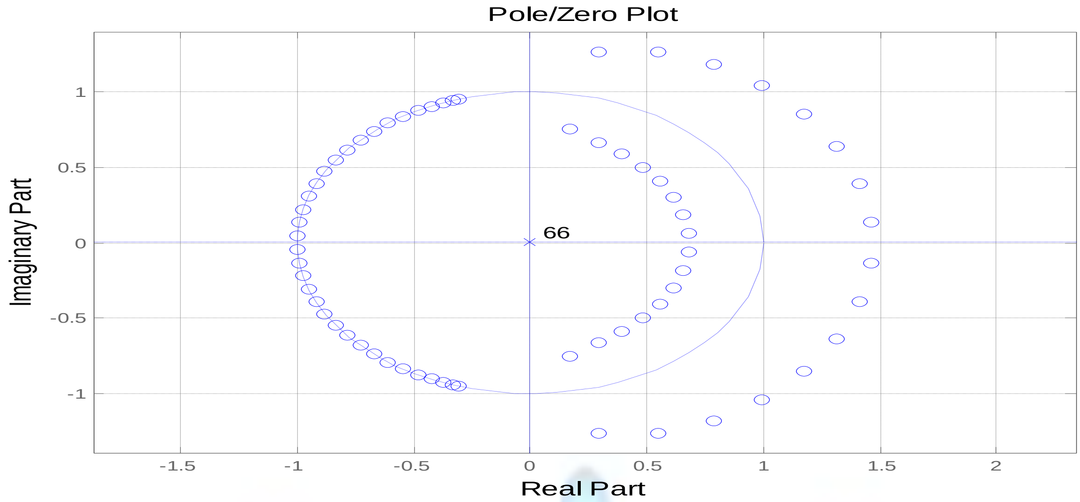
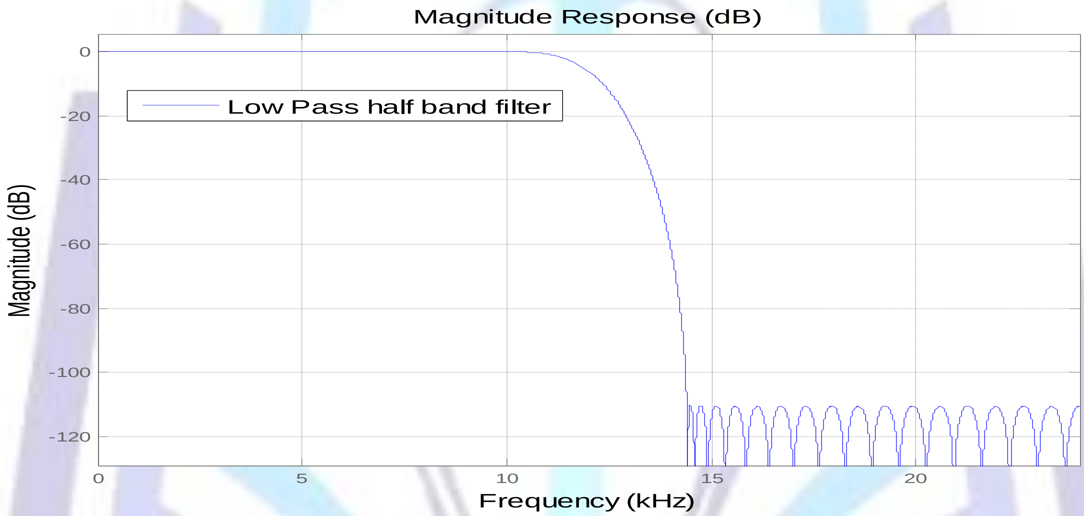
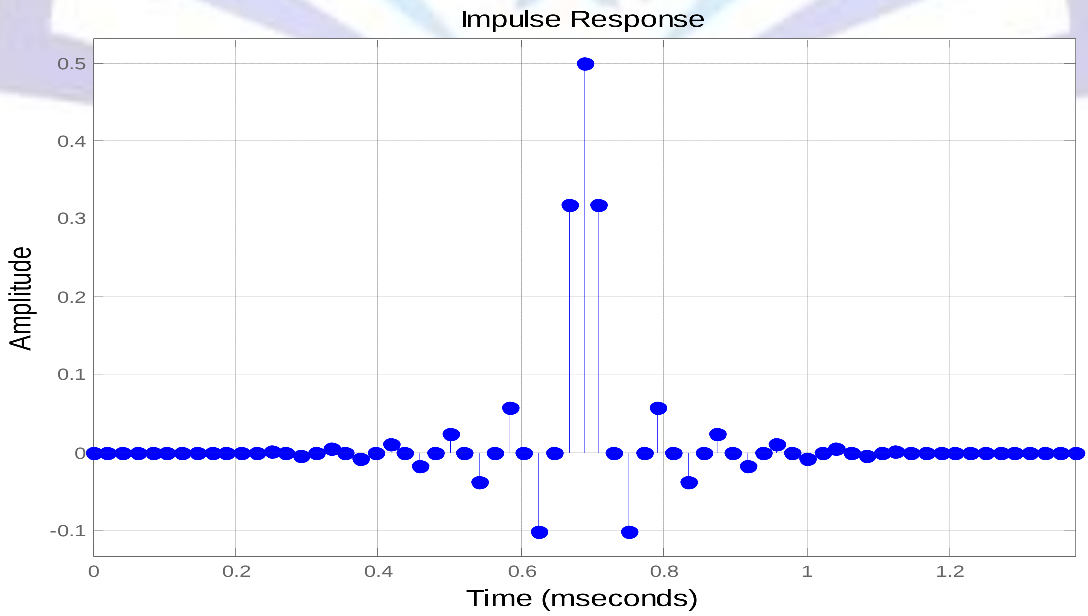



Fig 4: Output Responses of Equiripple Transposed FIR



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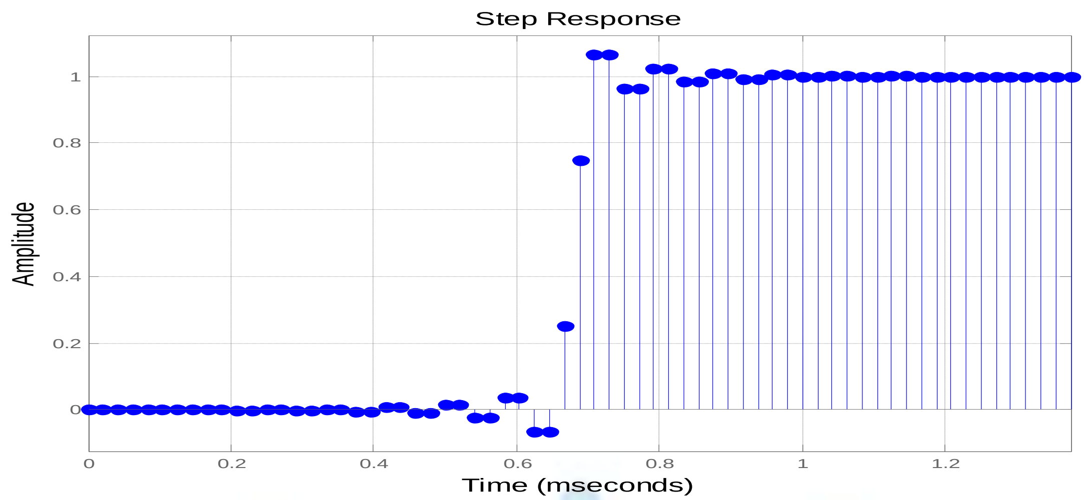


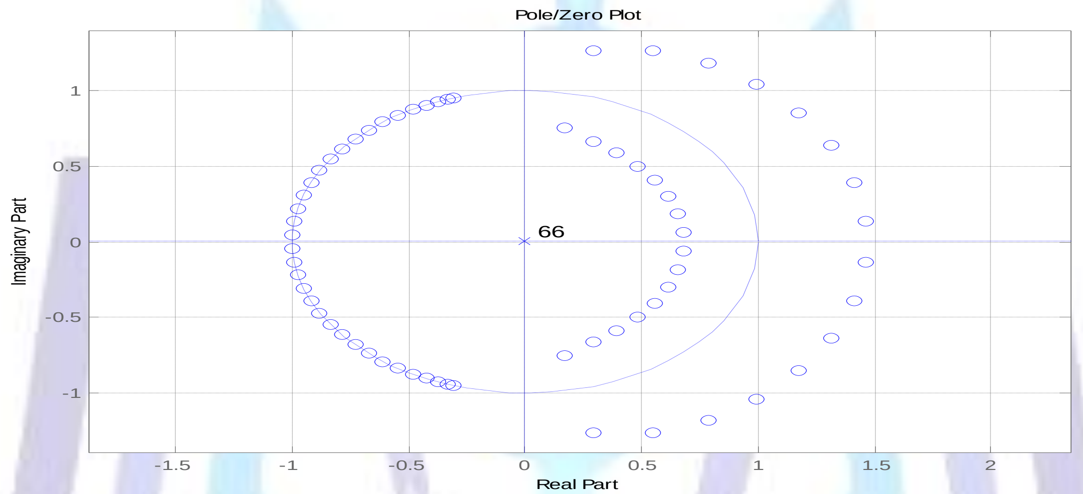


Fig 5: Various Output Response of Equiripple Symmetric FIR

The hardware requirements of both the designs have been calculated in terms of multipliers and adders to calculate the implementation cost. The performances of both designs are almost identical but their multipliers and multiplier per input sample cost varies greatly, as shown in Table 1. Required number of multipliers and multiplications per input sample in case of transposed form is 35 and for symmetric form is 18.

**Table 1. Implementation cost**

| DESIGN | MULT | ADD | MPIS | APIS |
|---|---|---|---|---|
| **Direct Form FIR Transposed** | **35** | **34** | **35** | **34** |
| **Direct Form symmetric FIR** | **18** | **35** | **18** | **35** |

## 6. CONCLUSION

In this paper, an optimized half band polyphase decomposition technique has been presented to implement the decimator for multirate applications. The proposed design has been implemented using transformed direct form and Symmetric direct form structures. The Symmetric direct form FIR filter has consumed 18 multipliers as compared to 35 in case of transposed direct form FIR filter to provide area efficiency. The proposed structure has also shown 50 % reduction in multiplications per input sample. So symmetric structure is well suited for cost effective implementation of decimator design.

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## Author’ biography

Mr. Rajesh Mehra is currently Associate Professor at National Institute of Technical Teachers’ Training & Research, Chandigarh, India. He is pursuing his PhD from Panjab University, Chandigarh, India. He has completed his M.E. from NITTTR, Chandigarh, India and B.Tech. from NIT, Jalandhar, India. Mr. Mehra has more than 16 years of academic experience. He has authored more than 125 research papers including more than 75 in Journals. Mr. Mehra’s interest areas are VLSI Design, Embedded System Design, Advanced Digital Signal Processing. Mr. Mehra is member of IEEE & ISTE.

Lajwanti Singh is currently Assistant professor at Anand International College of Engineering, Jaipur, India. She is pursuing her ME from Punjab University, Chandigarh, India. She has completed her B.E from RCEW, Jaipur, India. She has more than 7years of academic experience. Her interest areas are Digital Signal Processing, Microwave Engineering and VLSI Design.