DOI: https://doi.org/10.24297/ijct.v19i0.8123

Model-Based Parallelizer for Embedded Control Systems on Single-ISA Heterogeneous Multicore Processors

Zhaoqian Zhong[1],Masato Edahiro[2]

[1]Ph.D. candidate, Graduate School of Information Science, Nagoya University

[2]Professor, Graduate School of Informatics, Nagoya University

[1]zhaoqian@ertl.jp

Abstract

This paper presents a model-based parallelization approach to parallelize embedded systems on single-ISA heterogeneous multicore processors, especially processors with the ARM big.LITTLE architecture, wherein the core assignment of the Simulink blocks is determined based on the control design constraints and characteristics of the big.LITTLE architecture. The proposed approach uses a hierarchical clustering method on Simulink blocks to reduce the problem scale, and an integer linear programming (ILP) formulation to determine the core assignment solution, considering load balancing and minimization of inter-core communication across cores with different performances. Finally, we generate the parallel code of the model based on the core assignment solution for execution on the processors. We evaluate the proposed approach by comparing it with existing methods and generating the parallel code on a single-board computer with the big.LITTLE architecture to determine its effectiveness.

Keywords: Single-ISA heterogeneous multicore processor, ARM big.LITTLE architecture, model-based development, MATLAB Simulink, parallelization

1. Introduction

Recently, as embedded control systems such as automotive control systems are becoming larger and more complex, model-based development (MBD) with platforms such as MATLAB/Simulink [1] is becoming increasingly common. A Simulink model is a brief and descriptive block diagram that can be automatically translated to a sequential source code for embedded implementation on single-core processors. On the other hand, heterogeneous multicore processors of the single instruction set architecture (ISA) [2] have potential benefits over homogeneous multicore processors. On a single-ISA heterogeneous multicore processor, cores may execute the same instruction set; however, they offer different capabilities and performances, such as different clock frequencies and power consumption. The combination of these heterogeneous cores may lead to better application performance. To implement the control models described in Simulink on a single-ISA heterogeneous multicore processor, it is important to partition the generated control software based on control design constraints and parallelize the software components based on the characteristics of single-ISA heterogeneous multicore processors for parallel execution.

In this paper, a model-based parallelization approach is proposed to parallelize embedded systems built in the Simulink MBD environment on single-ISA heterogeneous multicore processors, especially processors with the ARM big.LITTLE architecture [3]. In this approach, a hierarchical clustering method is proposed to group blocks of the same attribute to top-level clusters. Then, we use an integer linear programming (ILP) formulation to assign these clusters on heterogeneous cores for the lowest communication cost and proper load balance. Our approach can also generate parallel codes, based on the core assignment solution for execution on the processor.

The contributions of our work are as follows.

CC BY

- We utilize SHIM [4] to estimate the workload of Simulink blocks and evaluate target processors in our approach. Hence, necessary parameters such as block execution time and signal line communication time can be easily acquired without executing the models on the processor in advance.

- An available ILP formulation is proposed to parallelize the model, considering minimization of the communication cost, load balancing, and the characteristics of single-ISA heterogeneous multicore processors.

- A new structure called a cluster is proposed in our work, where Simulink blocks are gathered based on user configuration or identical attributes. Since building ILP formulations directly on Simulink blocks may lead to a considerable number of ILP variables and constraints, and too long solver run-time in complex models, using clusters can reduce the problem scale significantly, which makes the ILP computation much faster in most cases.

- Our proposed approach also contains code generation and user feedback, where model designers can easily implement their models for execution on the processor and grasp how the models are parallelized in the MBD environment.

2. Related Work

There is a large amount of research being done on parallelizing control models in MBD, which can roughly be divided into code-level parallelization and model-level parallelization. For code-level parallelization, it is common to use tools such as MATLAB Coder [5] to generate sequential C codes from models and then use a parallel compiler [6, 7] to parallelize the generated C codes. Code-level parallelization can provide higher parallel performance thanks to more fine-grained parallelism than parallelization at block level. However, since the generated sequential C codes discard some of the control information, it is hard to parallelize the model due to control design constraints. In addition, it is difficult to extract block allocation results, for user feedback and model evaluation, in code-level parallelization. Meanwhile, for model-level parallelization [8, 9, 10], it is common to extract block-level parallelism from models, and partition these blocksto the cores on the processor. Since a Simulink model can be seen as a block diagram or a dataflow graph, which consists of blocks that represent different parts of a system, and signal lines that define the dependency between the blocks, the model-level parallelization problem is to find a mapping and scheduling of block execution and signal line communication which minimize the execution time of the block diagram on the target architecture. The mapping and scheduling of blocks are complex optimization problems, which need to be solved simultaneously to maximize the utilization of each core. In addition, the communication time between different cores must also be taken into account during the mapping and scheduling of blocks to minimize the execution time of the application. In this case, linear programming (LP) introduces an appropriate solution to solve such problems [9, 11]. We can describe Simulink models and target processors in a LP formulation and give it proper constraints, then use LP solvers to solve the formulation for the optimal solution. However, in a complex control model there may be a substantial number of Simulink blocks and signal lines, thus the LP solver may run for a long time to solve the parallel problem on the blocks [9]. So, when parallelizing a large-scale model, it is necessary to reduce the problem scale for proper solver time when building the LP formulation.

Furthermore, most of these existing studies target homogeneous multicore processors, where all cores have the same parameters. It is easier to parallelize a control model for homogeneous multicores, since designers do not have to consider diversity of performance or power consumption, which are identical for all cores. But, for a single-ISA heterogeneous multicore processor composed of cores of varying performances and complexities, it is more difficult to distribute the workload in a balanced manner while achieving high parallel performance [2]. Moreover, due to the diversity of the cores, the parallelization of blocks becomes a nonlinear problem; the workload and inter-core communication time caused by signal lines may change when blocks are allocated on different cores. Among the single-ISA heterogeneous multi-core architectures, we focus on architectures such as the ARM big.LITTLE architecture [3], where cores are grouped by their parameters and in

each group, cores are homogeneous except for the system core, if it exists. On a multi-core processor with the big.LITTLE architecture, cores are marked big or LITTLE due to their diversity. In this case, the inter-core communication can be described as a data transaction behaviour between the same type of cores, or between big and LITTLE cores, and it makes parallelization a typical LP problem. On a processor with the big.LITTLE architecture, we can describe this problem as minimizing the communication time to reduce the whole model execution time, while allocating blocks to big or LITTLE cores according to their workload; thus, it is possible to achieve considerably higher parallel performance and lower power consumption compared to using only homogeneous cores.

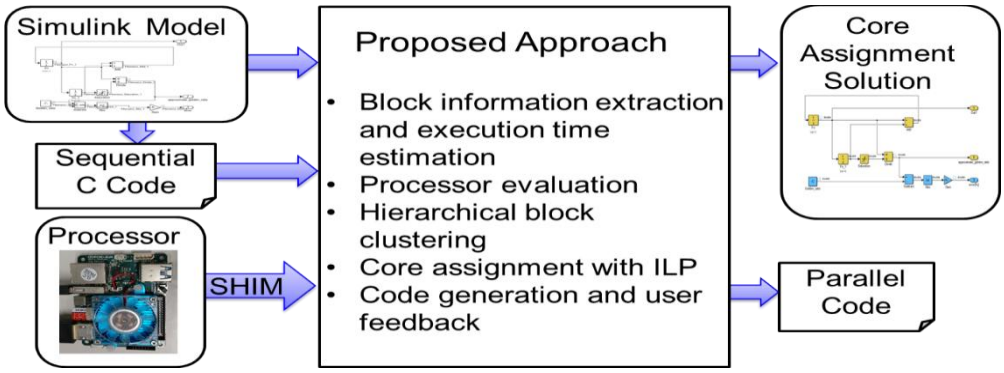


Fig. 1: Overview of model-levelparallelizationapproachin MBD for multicore processor

Fig. 1 shows an overview of our proposed approach for model-level parallelization. It solves the model-level parallelization problems for processors with the big.LITTLE architecture and generates static core assignment solution of the Simulink models. Compared to dynamic task allocation, static core assignment, such asILP [11] and graph partition [12, 13], is more suitable for embedded control applications, since static core assignment does not need to run a task scheduler to determine the execution of blocks, which leads to a much smaller overhead in the execution of the application. Also, a copy of the input model where the blocks are colored due to core assignment is generated as feedback to the model designers. With this graph, the model designers can grasp how the input models are partitioned on the target processor and improve the design of the input control models.

3. Proposed Approach

In this section, we present an overview of our proposed parallelization approach, which combines the characteristics of both control design and implementation design, to solve the parallelization problems for the big.LITTLE architecture. Our approach consists of the 4 phases in Fig. 2 and they are described in the following subsections.

- Data Extraction: extract information from the input Simulink model and the target processor and generate the necessary data file for parallelization.
- Hierarchical Clustering: group blocks according to user configuration and block attributes into high-level clusters.
- Core Assignment: assignment of the clusters to cores with our ILP formulation.
- Code Generation: generate the parallel code according to the core assignment solution.

3.1 Data Extraction

Our proposed approach takes control models designed in MATLAB Simulink, the hardware description of the target processor, and a user configuration file as the initial input. The user configuration file contains demands

from model designers regarding implementation, such as which cores on the processor should be utilized to parallelize the input model, or whether some special Simulink blocks are preferred to be assigned a specified core. We utilize tools from SHIM [4] to evaluate the target big.LITTLE heterogeneous multicore processors. SHIM is a hardware abstraction description standardized by Multicore Association [14], and it provides tools to roughly estimate software performance at the instruction level, so that we can easily understand how many clock cycles an instruction may take to be executed on a specified core. In our approach, we set the LITTLE core as the base core, and use SHIM tools to generate a SHIM data file which obtains some of the architectural characteristics, such as clock cycles for instructions on the base core. Also, we need to evaluate the processor for performance information such as communication overheads between different cores, and processing speeds of big and LITTLE cores.

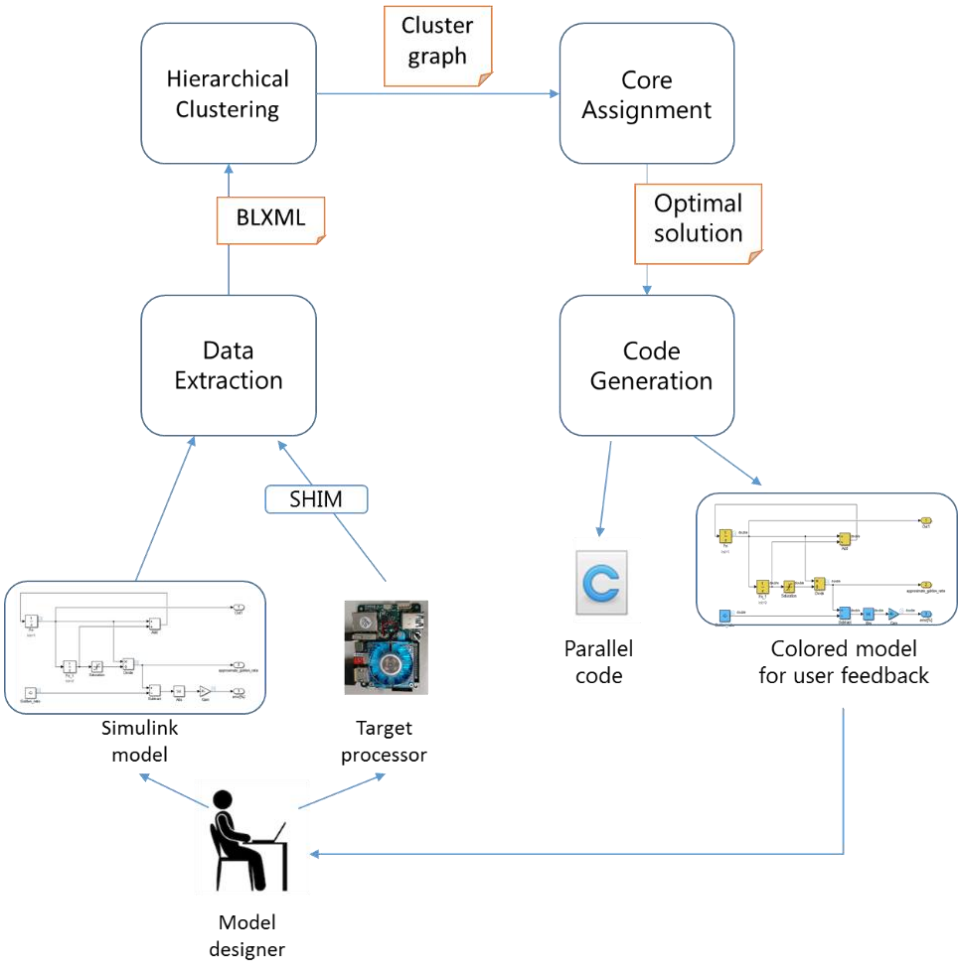
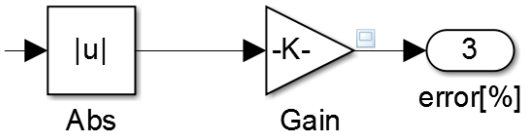


Fig. 2 Overview of each phrase in proposed approach

We standardize a block-level structure XML file (BLXML file) to describe the Simulink model in the proposed approach. The BLXML file mainly contains the following information, which is used in the next phase of our approach:

- Block parameters such as control rate, functional module, data type, etc.;
- Block dependency on other blocks;
- Initialization and execution code of each block;
- Estimated execution time of each block.

Block parameters can be obtained from the Simulink model file and block dependency can be extracted from the block diagram of the models. We generate a sequential C code of the input model with MATLAB Coder, and initialization and execution code of each block can be obtained from the generated code file. Execution time of each block can be estimated by combining block codes and instruction clock cycles in the SHIM data file. Fig. 3. a) shows a gain block in a Simulink model and Fig. 3. b) is the code of the gain block in the BLXML file.



a) Gain block in a Simulink block

```
<block blocktype="Gain" id="6" name="Gain" rate="-1">
  <input line="Abs_1" port="Gain_1">
    <connect block="Abs" port="Abs_1"/>
  </input>
  <output line="Gain_1" port="Gain_1" usename="true">
    <connect block="error" port="error_1"/>
  </output>
  <var line="Abs_1" mode="input" name="Abs_1" port="Gain_1" type="
   real_T"/>
  <var line="Gain_1" mode="extout" name="Gain_1" port="Gain_1" type="
   real_T"/>
  <param name="Gain_Gain" storage="P" type="real_T"/>
  <code file="Fibonacci.c" line="76" type="task">
                Gain_1 = P.Gain_Gain * Abs_1;
  </code>
  <code file="Fibonacci.c" line="113" type="init">
                Gain_1 = 0.0;
  </code>
  <code file="data.c" line="36" type="param">
                0.61803398874989479
  </code>
  <performance best="12.5" type="task" typical="16.5" worst="22.5"/>
  <performance best="12.75" type="init" typical="12.75" worst="12.75"/
   >
  <forward block="error" type="port">
    <var line="Gain_1" mode="input" name="Gain_1" port="error_1" type=
     "real_T"/>
  </forward>
  <backward block="Abs" type="data">
    <var line="Abs_1" mode="output" name="Abs_1" port="Abs_1" type="
     real_T"/>
  </backward>
</block>
```

b) Code of gain block in BLXML file

Fig. 3 A sample ofSimulink block and BLXML file

3.2 Hierarchical Clustering

In this phase, we group the blocks of the Simulink models, based on the characteristics of control design on different levels, into clusters to reduce the ILPproblem scale.

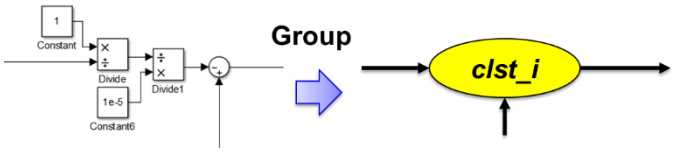


Fig. 4Grouping continuous blocks into a cluster

First, we group the Simulink blocks that should be assigned to the same core according to user configuration. Then, some of the blocks should be intentionally grouped and assigned to the same core for design and implementation optimization. From the point of view of model design, If blocks or Switch Case blocks are used when execution of some blocks is determined by a single input signal, and blocks on the branches between an If block or Switch Case block and the corresponding merge block can be grouped to avoid branch selection. Also, from the point of view of implementation, blocks such as Data Store Read blocks or Data Store Write blocks are used to read or write values to the same memory, and it is desirable to group blocks that are between a pair of Data Store Read block and Data Store Write block to reduce memory access. Moreover, continuous blocks which have a direct connection and share the same attribute should be clustered. For example, if two continuous blocks belong to the same functional module in the control design, in the model they are usually gathered to the same atomic subsystem and they should not be separated to different cores in the core assignment. Also, if two blocks have a signal line in between and share the same rate parameter, they have a similar iterative execution behaviour and can be seen as only one unit in core assignment.Fig. 4 shows an example of grouping continuous blocks with the same attribute into a cluster. We do such clustering hierarchically and the final generated block groups are called clusters in our approach. Since ILP is a rigorous but heavy method for optimization problem, parallelizing blocks directly may lead to a substantial number of ILP variables and constraints, and the solver may run for a very long time to obtain the optimal solution. Meanwhile, utilization of clusters instead of blocks in ILP greatly reduces the scale of the ILP problem to avoid too long a solver time. In actual scenarios, there are commonly several tens of clusters that have the same control rate and belong to the same functional module in an automotive control model [15].

3.3 Core Assignment

In this phase we assign clusters to cores on the target multicores. In order to define the model in the ILP formulation, we first generate a cluster graph from the result of the hierarchical clustering and estimate the necessary data from the BLXML file. Then, we fit the forced core assignment according to the user configuration file and assign other clusters to cores with our ILP formulation. This phase is extremely important in our proposed approach, so we provide more details about the proposed algorithm using ILP formulation in the next section. Then, we expand the clusters to the Simulink blocks and assign the blocks to the cores on the target processor. Since our approach supports models with multiple control rates and action subsystems, where If or Switch Case blocks are used, it is important to ensure that these Simulink blocks will be executed in the right order, or it may lead to a fatal error in the code generation phase. We perform a path analysis on the block dependency to determine the execution sequence of the blocks on each core. Finally, we generate a copy of the input model where the blocks are colored according to the core assignment solution to tell the model designer the core to which these blocks are assigned.

3.4 Code Generation

In the last phase we generate the parallel code of the input model from the core assignment solution and the BLXML file. The generated code is implemented in POSIX Threads. First, the block diagram of the input model is translated into a graph, based on the CSP (communicating sequential processes) [16] theory, due to the path analysis result, where the block dependency and execution order can be easily distinguished. We create one thread for each given core on the target processor, then write the execution code of each block from the BLXML file to the threadsaccording to the core assignment solution and their execution order in the CSP graph. Execution cores for threads are specified using pthread affinity.

4 ILP Formulation for Core Assignment

In this section, we present our ILP formulation for cluster-level core assignment on heterogeneous multicore processors with the big.LITTLE architecture. Given the cluster graph, the user configuration, and the parameters of the target processor, our ILP formulation discovers the optimal static core assignment solution, which aims at minimizing the communication transactions between cores to reduce the overall application execution time. In addition, our ILP formulation distributes the workload of the clusters to each given core due to the characteristics of the big.LITTLE architecture.

4.1 Architecture Definition

In our formulation, the user should specify which cores on the processor are used to parallelize the input model in the user configuration file; the parallelization problem on heterogeneous multicore processors with the big.LITTLE architecture is to find the mapping of clusters on the given cores. In order to solve this problem using linear programming, we divide the target heterogeneous multicore processor into two levels: core groups and cores. In our formulation, the cores in the big.LITTLE architecture are grouped into the big group and the LITTLE group by their performance. We evaluate some of the major products in the big.LITTLE architecture, such as Odroid-XU4 [17] and Jetson TX2 [18] and observe that the communication overheads between two big cores or two LITTLE cores always stay at a very close range, while the overhead between a big core and a LITTLE core does the same. Therefore, in our ILP formulation we assume that the inter-group overheads between cores of different core groups are the same, and in both core groups the inter-core overhead is also the same.

At the core group level, we define the set of 2 core groups as $GROUP = \{core\_group_g | g \in [big, LITTLE]\}$. Each core group is defined as a 3-tuple, $core\_group_g = (core\_group\_num_g, core\_overhead_g, CORE_g)$, where $core\_group\_num_g$ represents the number of cores in $core\_group_g$,$core\_overhead_g$ denotes the overhead of communication in $core\_group_g$, and $CORE_g$ is the set of cores in $core\_group_g$. We use the communication overhead between a big core and a LITTLE core as the communication overhead between core groups and it is denoted by$group_overhead$.

At the core level $CORE_g = \{core_{p,g} | p \in [0, core\_group\_num_g - 1]\}$ defines the set of cores in either core group. A core is defined as a 5-tuple, $core_{p,g} = (core\_clst\_cpu\_util_{p,g}, core\_util_{p,g}, core\_speed_{p,g}, core\_max\_cpu\_util_{p,g}, core\_min\_cpu\_util_{p,g})$, where $core\_clst\_cpu\_util$ represents the total workload of clusters assigned to this core in the core assignment solution, $core\_util$ represents the utilization ratio of the core to be used in our formulation, and$core_speed$ represents the processing speed of this core. The value of$core_util$ is specified in the user configuration if factors such operating system (OS) influence the utilization of the core, and its default value is set to 1 where all of the core resources can be used. The value of $core\_speed$ should be given in the user configuration or extracted from the evaluation on the real processor. In order to distribute the workload to each core, we use $core\_max\_cpu\_util_{p,g}$ and $core\_min\_cpu\_util_{p,g}$ as the maximum and minimum of the cluster workload assigned to $core_{p,g}$, and they are supposed to be taken from the user configuration file if the model designer prefers to balance the block distribution. In this paper, we set $core\_min\_cpu\_util = 1$ to ensure that all of the cores are used and $core\_max\_cpu\_util = total\_cpu\_util / (\sum_{g \in GROUP} (\sum_{p \in CORE_g} core\_speed_{p,g})) * (1.05 + t)$, where $total\_cpu\_util$ denotes the sum of all the blocks' estimated execution time and t denotes a value to avoid a non-optimal solution. Since it is possible that the constraint on $core_max_cpu_util$may not be satisfied and the formulation may not be solved, t is used to increase the value of $core\_max\_cpu\_util$ if the proposed ILP formulation fails to find any solution.

4.2 Model Definition

After hierarchical clustering, the input model is represented by a cluster graph, which is an acyclic directed graph $G = (CLST, CONN)$, where $CLST$ is the set of clusters and $CONN$ is set of the communication edges between the clusters.

The number of clusters is denoted by m and the set of m clusters is defined as $CLST = \{clst_i | i \in [0, m-1]\}$. Each cluster is defined as $clst_i = (clst\_cpu\_util_i)$, where $clst\_cpu\_util_i$ is the estimated workload of the cluster $clst_i$. The estimated workload $clst\_cpu\_util$ is decided by the sum of estimated execution time and the control rate of the blocks grouped to $clst_i$. From the BLXML file we can find the estimated execution time and the control rate parameter of the blocks. The sum of the estimated execution times shows how long it takes to execute all blocks in this cluster sequentially on the base core of the processor and the control rate parameter determines how frequently the cluster is executed in loop interactions. For example, a very low control rate shows that the blocks in this cluster are not executed frequently, so even if the sum of the estimated execution times of the blocks in this cluster is large, its $clst\_cpu\_util$ may be still very small. We find the cluster with the lowest control rate $clst\_lowest\_rate$, and use $clst\_execution\_time_i$ to denote the sum of estimated execution times of the blocks grouped to $clst_i$ and $clst\_rate_i$ to denote the control rate of the blocks grouped to $clst_i$. Hence, the estimated workload of $clst_i$ is defined as $clst\_cpu\_util_i = clst\_execution\_time_i * clst\_rate_i / clst\_lowest\_rate$.

The number of communication edges is denoted by n. We define the set of n communication edges as $CONN = \{conn_j | j \in [0, n-1]\}$. Each communication edge is defined as a 3-tuple $conn_j = (conn\_s\_clst_j, conn\_t\_clst_j, conn\_weight_j)$, where $conn\_s\_clst_j$ and $conn\_t\_clst_j$ represent the start cluster and termination cluster of communication edge $conn_j$, and $conn\_weight_j$ is the estimated communication time of a communication edge. A communication edge can be seen as the set of signal lines which start from blocks in $conn\_s\_clst_j$ and go to blocks in $conn\_t\_clst_j$, so the $conn\_weight_j$ is decided by the signal line number and the control rates of $conn\_s\_clst_j$ and $conn\_t\_clst_j$. For example, a signal line from a block in $conn\_s\_clst_j$ to a block in $conn\_t\_clst_j$ means the two clusters have a communication transaction, and either $conn\_s\_clst_j$ or $conn\_t\_clst_j$ having very high control rates means that this communication transaction behaviouroccurs very frequently in loop interactions, and $conn\_weight_j$ should be set a high value accordingly. In our formulation, the value of $conn\_weight_j$ is set to the product of the number signal lines between $conn\_s\_clst_j$ and $conn\_t\_clst_j$ and the higher of the control rate multiples of $conn\_s\_clst_j$ and $conn\_t\_clst_j$ to quantize the communication behaviourof $conn_j$.

4.3 Variables

Following are the variables used in our ILP formulation to denote to which core group or core a cluster is assigned:

- $x\_group_{i,g}$: equal to 1 if cluster $clst_i$ is assigned to core group $core\_group_g$ and equals to 0 if not.
- $x\_core_{i,p,g}$: equal to 1 if cluster $clst_i$ is assigned to core $core_{p,g}$ in group $core\_group_g$ and equal to 0 if not.

We also use the following variables in our ILP formulation to denote whether both end clusters of a communication edge are assigned to the same core group or to the same core:

- y_group_j: equal to 0 if both end cluster $conn\_s\_clst_j$ and $conn\_t\_clst_j$ of communication edge $conn_j$ are assigned to the same group and equal to 1 if not.
- $y\_core_{j,g}$: equal to 0 if both end cluster $conn\_s\_clst_j$ and $conn\_t\_clst_j$ of communication edge $conn_j$ are assigned to the same core in group $core\_group_g$ and equal to 1 if not.

4.4 Objective Function

Our proposed ILP formulation assigns clusters to the specified cores on a heterogeneous multicore processor with the big.LITTLE architecture. For all communication edges, $conn_j$, whose $y\_group_j = 1$ or $y\_core_{j,g} = 1$, we use the product of $conn\_weight_j$ and the corresponding overhead as the communication cost of $conn_j$. So, the sum of all these communication costs represents the communication cost of the whole application and we can

minimize this communication cost to reduce both the number of communication edges and the communication time between cores. The objective function for the core assignment problem is as follows:

$$minimize \sum_{j \in CONN} conn\_weight_j * (y\_group_j * group\_overhead + \sum_{g \in GROUP} y\_core_{j,g} * core\_overhead_g)$$

4.5 Constraints

The constraints for the core assignment problem are defined as follows.

- Each cluster shall be assigned to only one core group:

$$\forall \boldsymbol{i} \in \boldsymbol{CLST}: \sum_{\boldsymbol{g} \in \boldsymbol{GROUP}} \boldsymbol{x\_group_{i,g}} = \boldsymbol{1} \quad (1)$$

- Each cluster shall be assigned to only one core on the processor:

$$\forall \boldsymbol{i} \in \boldsymbol{CLST}: \forall \boldsymbol{g} \in \boldsymbol{GROUP}: \sum_{\boldsymbol{p} \in \boldsymbol{CORE_g}} \boldsymbol{x\_core_{i,p,g}} = \boldsymbol{x\_group_{i,g}} \quad (2)$$

- Whether the two end clusters of a communication edge are assigned on the same core group is calculated as follows:

$$\forall \boldsymbol{j} \in \boldsymbol{CONN}: \boldsymbol{y\_group_j} = (\sum_{\boldsymbol{g} \in \boldsymbol{GROUP}} \boldsymbol{abs}\left(\boldsymbol{x\_group_{conn\_t\_clst_j,g}} - \boldsymbol{x\_group_{conn\_s\_clst_j,g}}\right)) \quad (3)$$

- Whether the two end clusters of a communication edge are assigned on the same core is calculated as follows:

$$\forall \boldsymbol{j} \in \boldsymbol{CONN}: \forall \boldsymbol{g} \in \boldsymbol{GROUP}: \boldsymbol{y\_core_{j,g}} = \left\lfloor (\sum_{\boldsymbol{p} \in \boldsymbol{CORE_g}} \boldsymbol{abs}\left(\boldsymbol{x\_core_{conn\_t\_clst_j,p,g}} - \boldsymbol{x\_core_{conn\_s\_clst_j,p,g}}\right))/\boldsymbol{2} \right\rfloor \quad (4)$$

- The sum workload of clusters assigned to each core of different processing speed is calculated as follows:

$$\forall \boldsymbol{g} \in \boldsymbol{GROUP}: \boldsymbol{p} \in \boldsymbol{CORE_g}: \boldsymbol{core\_clst\_cpu\_util_{p,g}} = \sum_{\boldsymbol{i} \in \boldsymbol{CLST}} \boldsymbol{x\_core_{i,p,g}} * \boldsymbol{core\_util_{p,g}} / \boldsymbol{core\_speed_{p,g}} \quad (5)$$

- Sum workload of clusters assigned to a core shall not exceed its upper limit:

$$\forall \boldsymbol{g} \in \boldsymbol{GROUP}: \boldsymbol{p} \in \boldsymbol{CORE_g}: \boldsymbol{core\_clst\_cpu\_util_{p,g}} \leq \boldsymbol{core\_max\_cpu\_util_{p,g}} \quad (6)$$

- Sum workload of clusters assigned to a core shall not exceed its lower limit:

$$\forall \boldsymbol{g} \in \boldsymbol{GROUP}: \boldsymbol{p} \in \boldsymbol{CORE_g}: \boldsymbol{core\_clst\_cpu\_util_{p,g}} \geq \boldsymbol{core\_min\_cpu\_util_{p,g}} \quad (7)$$

5 Experiments

To study the scalability and efficiency of our method with the ILP formulation, we utilize randomly generated cluster graphs with different number of clusters. Furthermore, we parallelize an automotive control evaluation model based on real scenarios with our approach and execute the parallel code on ODROID XU4 single-board computers. Among a variety of ILP solvers, we use IBM ILOG CPLEX Optimization Studio [19] to solve the core

assignment problem. The upper time limit of CPLEX execution time is acceptably set to 5 hours (18,000 seconds), even though it takes only a few minutes to find the solution for our formulation of 100 clusters with CPLEX. The proposed approach and the CPLEX solver are run on a PC with an Intel Xeon CPU E5-2695v2 2.40GHz, in which the cache size is 30720 kB and the main memory size is 32 GB.

5.1 Randomly Generated Cluster Graphs

We use randomly generated directed acyclic graphs of clusters to evaluate the performance of the ILP formulation for the assignment of cores. Although we should use data from real control models, it is not easy to gather reasonable models, and it is also difficult to artificially generate well-controlled models. Hence, we use randomly generated DAGs, such as input cluster graphs, whose parameters, such as cluster estimated workload and communication time, are generated randomly. The ranges of these parameters are based on real-scenario models.

Table 1. Core assignment on randomly generated cluster graphs for 1 big and 1 LITTLE cores.

Clusternumber	Approach	Average solver time	Average speedup	Average load balance
20	proposed	0.13	2.88	1.90
	khmetis	1.51	1.65	1.37
30	proposed	0.22	3.23	1.91
	khmetis	3.66	1.74	1.34
40	proposed	0.19	3.34	1.90
	khmetis	6.55	1.76	1.33
50	proposed	0.13	3.44	1.89
	khmetis	10.26	1.78	1.33
60	proposed	0.32	3.50	1.88
	khmetis	14.60	1.78	1.33
70	proposed	0.32	3.52	1.86
	khmetis	19.66	1.76	1.32
80	proposed	0.31	3.57	1.87
	khmetis	25.37	1.78	1.32
90	proposed	0.46	3.56	1.86
	khmetis	31.75	1.75	1.31
100	proposed	0.60	3.56	1.86
	khmetis	38.99	1.81	1.34

In these experiments, we generate 100 cluster graphs of each specified cluster number, then use our ILP formulation and a graph partition method called khmetis [20] on them for core assignment solutions. khmetis is a program provided by hMETIS [21], and it computes a k-way partitioning using multilevel k-way partitioning. hMETIS is commonly used to solve problems such as task allocation for multicores [8]. Since khmetis uses random seeds to generate graph partitions, we execute khmetis 100 times with different execution parameters and use the partition with the lowest communication cost as the core assignment result in our experiments. We assume abig.LITTLE heterogeneous multicore system as the target processor, where *cspeed* of big cores is 3 times higher than *cspeed* LITTLE cores and *dmaf* times higher than *cdma*. We use a user configuration of 1 big core and 1 LITTLE core, and another of 2 big cores and 4 LITTLE cores in our experiments.

We present metrics on the core assignment results of randomly generated cluster graphs in Table 1 and Table 2. Average solver time denotes the average execution time required by our ILP formulation and khmetis to solve core assignment problems of different sizes. Average speedup metric is the ratio of the sequential execution time and the parallel execution time at the cluster level. Here, we use the sum of the workload of all the clusters as the sequential execution time, and the parallel execution time is the total execution time computed by the core assignment result and the dependency of these clusters. Average load balance metric is the ratio between the sequential execution time and the highest *cdma* and it indicates whether the cores are used efficiently.

Table 2. Core assignment on randomly generated cluster graphs for 2 big and 4 LITTLE cores.

Clusternumber	Approach	Average solver time	Average speedup	Average load balance
20	proposed	14.14	3.01	3.52
	khmetis	36.97	1.82	3.19
30	proposed	1.88	4.25	4.72
	khmetis	40.54	2.96	3.70
40	proposed	8.30	5.16	5.38
	khmetis	45.17	3.89	4.09
50	proposed	9.94	6.16	5.56
	khmetis	50.61	4.42	4.20
60	proposed	22.07	6.67	5.60
	khmetis	57.93	4.59	4.27
70	proposed	54.2	6.91	5.61
	khmetis	66.09	4.77	4.34
80	proposed	89.23	6.91	5.60
	khmetis	75.77	4.70	4.37
90	proposed	214.58	7.15	5.6

	khmetis	89.86	4.74	4.37
100	proposed	462.91	7.03	5.59
	khmetis	102.24	4.67	4.40

For a small number of clusters and cores, our ILP formulation executes much faster than khmetis to obtain the solution. However, when the number of clusters and cores increase, the solver time to solve the core assignment problem in ILP may become much longer, while remaining within the acceptable upper time limit. Since the existing method khmetis cannot balance the weights of partitions well on heterogeneous architectures, it fails to parallel these clusters and cannot use cores more efficiently, with respect to the speedup and load balance, than ILP. However, for a smaller number of clusters on 6 cores, the ILP formulation may generate solutions of lower speedup and load balance compared to a larger number of clusters. Since we set the upper limit of cluster workload on each core, it is hard to distribute the cluster workload evenly in a scenario where the number of clusters is small but the workload of most clusters is large. In such cases, we raise the upper limit on the cores to generate a legal solution of poor workload balance, where most heavy clusters are assigned to big cores. Also, we use *comm* to the lower limit of workload on each core in the ILP formulation in order to utilize each given core, but for a small number of clusters this action may lead to too many communication transactions between cores and increase the whole application execution time.

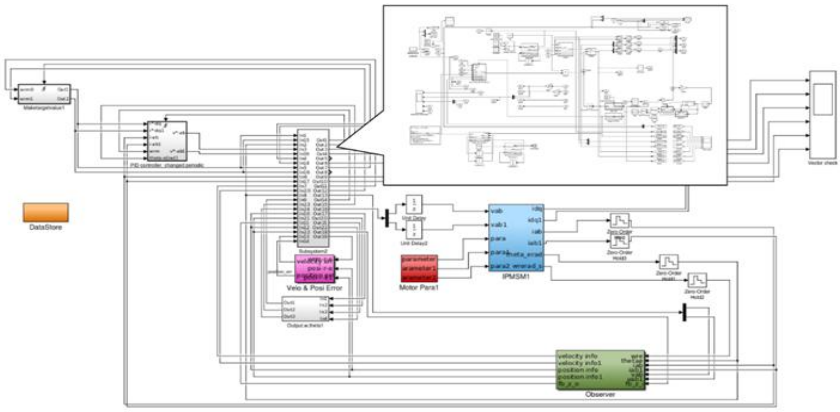


Fig. 5 Motor control model

5.2 Motor Control Model

The motor control model is abstracted from a real automotive control evaluation model. Fig. 5 provides an overview of the motor control model. This model is a multi-rate Simulink model and contains complex Simulink structures such as triggered subsystems and S-functions. The number of Simulink blocks in the motor control model is 514, and after hierarchical clustering, the number of clusters is 31 and the number of communication edges is 83. In this experiment, we perform parallelization on the motor control model with our approach and implement it on the Odroid-XU4 [16] board to evaluate the execution time of the generated parallel code with the core assignment solution from our ILP formulation. ODROID-XU4 is one of the latest single board computing devices and equips a Samsung Exynos 5422 processor which includes four Cortex-A15 and four Cortex-A7 cores in a big.LITTLE configuration as shown in Fig. 6. Ubuntu 16.04.3 is run on Odroid-XU4, and we set the CPUFreq Governor policy to performance mode to make sure the cores work at the highest clock frequency, where Cortex-A15 is at 2 GHz and Cortex-A7 is at 1.4 GHz. From the performance evaluation of the big cores and the LITTLE cores, we set the LITTLE cores as the base cores and *speed* the big cores is set to 2.2 times that of *speed* the LITTLE cores. Although we observe the execution time may suffer from influences, such as OS or TDP limit, *cost* each core is set to 1. We input the motor control model and the description file of Odroid-XU4 to our proposed approach and generate the core assignment solutions and the parallel codes for the specified configurations. Considering the number of clusters in the motor control model,

we use at most 4 cores in the experiment. We execute each of these generated parallel codes on the Odroid-XU4 board and record the execution times. Our approach takes only several minutes to generate these parallel codes.

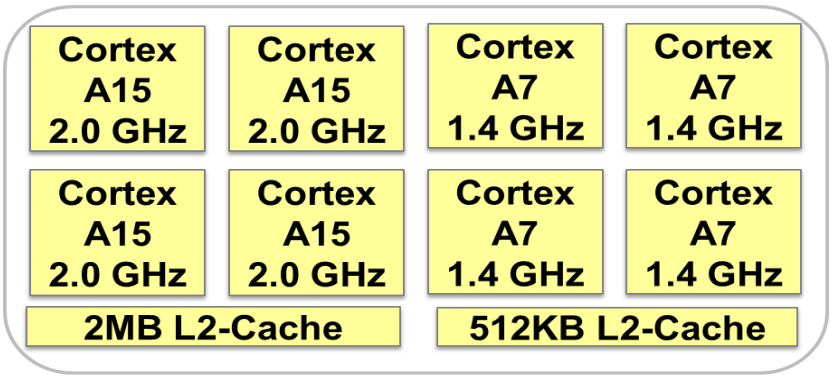


Fig. 6 Overview of Odroid-XU4

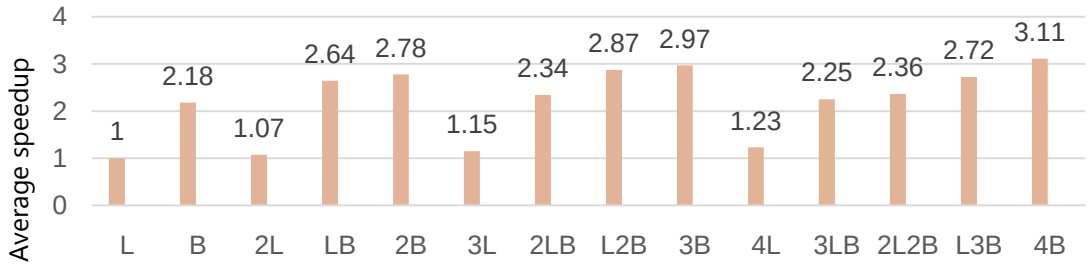


Fig. 7Speedup performance of generated codes executed on ODROID-XU4

Fig. 7 shows the speedup performance of generated codes of different configurations to be implemented on ODROID-XU4. L and B in the configuration name mean how many LITTLE cores or big cores are used to execute the generated parallel codes. We record the average execution time it takes to finish running the generated source code on ODROID-XU4 in seconds, and the average speedup is the ratio of the average execution time on a LITTLE core and the average execution time of the given configurations.

As shown by the results, although the execution on ODROID XU4 shows lower speedup than randomly generated cluster graphs in 5. 1, where speedup is calculated ideally at the cluster level, the core assignment in the configurations with both big and LITTLE cores achieves a decrease in application execution time and reasonable speedup, compared to configurations where the same type of core is used. This shows, for a control model of this size, our approach achievesreasonably high parallel efficiency and low communication cost on such processors in a short solver time.

However, in the result we observe that in some configurations it takes more time to execute the model when using more cores. For example, when using 2 big and 2 LITTLE cores, the speedup is lower than when using 2 big cores and only 1 LITTLE core. This is because when using more LITTLE cores, there are more signal lines across big and LITTLE cores, and these signal lines may lead to more heavy inter group communication during the execution and the whole execution time of the application will increase. Also, the motor control model is a multirate model based on real scenarios; most of its blocks have higher control rates and only a few blocks have a lower control rate. Due to workload constraints in our ILP formulation, if too many LITTLE cores are used for implementation, some high rate blocks are assigned to these slow cores and the threads on the LITTLE cores may suffer much longer execution time and result in a lower speedup. We observe that when using both big and LITTLE cores, using 1 LITTLE core and 2 big cores is the best choice to implement the

motor control model. In this configuration, most of the low rate blocks are assigned to the LITTLE core while heavy blocks are distributed to the 2 big cores to be executed in a well parallelized manner.

This shows a potential utilization of our approach when multiple models need to be executed on a processor simultaneously. By merging multiple models into 1 cluster graph while avoiding blocks from different models grouping into the same cluster, our approach can find the optimal solution to parallelize these blocks on the heterogeneous cores while keeping the execution time of the models and the utilization of cores optimal. However, it also leads to a challenge in parallelizing a Simulink model on a single-ISA heterogeneous multicore processor with the big.LITTLE architecture: when given several cores of different performances on a processor to implement a control model, it is possible that using only some of the given cores achieves the best parallel performance, but proper prediction is necessary in building the ILP formulation.

6 Conclusions

In this paper, we addressed a model-based parallelization approach, based on ILP, to parallelize embedded control systems designed on the MATLAB/Simulink platform for single-ISA heterogeneous multicore processors, especially processors with ARM big.LITTLE architecture. Compared to existing methods, our method can minimize the communication cost across cores to generate a better parallelization solution, while the workload of the input Simulink blocks can be distributed to cores of different performances. Moreover, our approach utilizes the characteristics of the ARM big.LITTLE architecture to achieve high parallel efficiency and core utilization. Results on randomly generated data have shown that a higher speedup and a lower communication cost are achieved by our approach on assumed architectures. We also implement a real model on the ODROID-XU4 board and observe a reasonable speedup performance. Besides the ARM big.LITTLE architecture, our ILP formulation can also be applied to other Single-ISA heterogeneous multi-core architectures, where cores can be grouped to heterogeneous clusters by inter-core communication overhead, and available cores in each cluster share inter-core communication overhead at close range. In future work, we plan to extend our approach to architectures where cores have more complicated communication behaviors.

Conflicts of Interest

The authors declare no conflicts of interest associated with this manuscript.

Acknowledgments

This work was supported by JSPS KAKENHI Grant Number 16H02800.

References

1. 5. MathWorks, Inc. "Simulation and Model-Based Design."https://jp.mathworks.com/products/simulink.html, 2015.

2. Kumar, Rakesh, et al. "Single-ISA heterogeneous multi-core architectures: The potential for processor power reduction." Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture. IEEE Computer Society, 2003.

3. Chung, Hongsuk, Munsik Kang, and Hyun-Duk Cho. "Heterogeneous Multi-Processing Solution of Exynos 5 Octa with ARM® big. LITTLE™ Technology." Samsung White Paper (2012).

4. Gondo, Masaki, Fumio Arakawa, and Masato Edahiro. "Establishing a standard interface between multi-manycore and software tools-SHIM." COOL Chips XVII, 2014 IEEE. IEEE, 2014.

5. MathWorks, Inc."MATLAB CoderGenerate C and C++ code from MATLAB code." https://jp.mathworks.com/
products/matlab-coder.html, The MathWorks, Inc, 2012.

6. Dan, Umeda, Youhei, Kanehagi,et al. "Automatic Parallelization of Designed Engine Control C Codes by MATLAB/Simulink. " Journal of Information Processing, Vol.55, No.8, pp 1817-1829, 2014.

7. Cha, Minji, et al. "Deriving high-performance real-time multicore systems based on simulink applications." Dependable, Autonomic and Secure Computing (DASC), 2011 IEEE Ninth International Conference on. IEEE, 2011.

8. Kumura, Takahiro, et al. "Model based parallelization from the simulink models and their sequential C code." Proceedings of the 17th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI 2012). 2012.

9. Höttger, Robert, Lukas Krawczyk, and BurkhardIgel. "Model-based automotive partitioning and mapping for embedded multicore systems." International Conference on Parallel, Distributed Systems and Software Engineering. Vol. 2. No. 1. 2015.

10. Yi, Ying, et al. "An ILP formulation for task mapping and scheduling on multi-core architectures." Proceedings of the conference on design, automation and test in Europe. European Design and Automation Association, 2009.

11. Tuncali, CumhurErkan, Georgios Fainekos, and Yann-Hang Lee. "Automatic Parallelization of Simulink Models for Multi-core Architectures." High Performance Computing and Communications (HPCC), 2015 IEEE 7th International Symposium on Cyberspace Safety and Security (CSS), 2015 IEEE 12th International Conferen on Embedded Software and Systems (ICESS), 2015 IEEE 17th International Conference on. IEEE, 2015.

12. Sou, Aburadani, and Masato,Edahiro. "Task Mapping Method for Hierarchical Many-core Processor Architectures." Journal of Information Processing, Vol.56, No.8, pp 1568-1581, 2015.

13. Edahiro, Masato, and Takeshi, Yoshimura. "New placement and global routing algorithms for standard cell layouts." Design Automation Conference, 1990. Proceedings., 27th ACM/IEEE. IEEE, 1990.

14. Multicore Association. "SHIM - Multicore Association." https://www.multicore-association.org/workgroup/shim.php, 2018.

15. Embedded Multicore Consortium.Discussion at Embedded Multicore Consortium, 2015.

16. Hoare, Charles Antony Richard. "Communicating sequential processes." Communications of the ACM 21.8 (1978): 666-677.

17. Hardkernel. ”ODROID-XU4 User Manual.” http://www.hardkernel.com, 2017.

18. Franklin, D. "NVIDIA Jetson TX2 Delivers Twice the Intelligence to the Edge." NVIDIA Accelerated Computing| Parallel Forall (2017).

19. CPLEX, IBM ILOG. "12.7, User’s Manual for CPLEX." CPLEX division, 2016.

20. Karypis, George, and Vipin Kumar. "Multilevelk-way partitioning scheme for irregular graphs." Journal of Parallel and Distributed computing 48.1 (1998): 96-129.

21. Karypis, George. "hMETIS 1.5: A hypergraph partitioning package." http://www.cs.umn. edu/~ metis, 1998.